Model	Date	CHANGE LIST
ZGL REV:A	2/16	1. FIRST RELEASED
ZGL REV:B	3/16	1. Del R21309 and stuff R67240 for power sequence 2. Add D13095 for GPU_THROTTING# issue 3. Add TVS on HDMI/DP port for MB L&L 4. Stuff R20825/R20828 for EA fail 5. Change Subwoofer ALC105 to ALC1006 for Design change 6. Add & reverse HDD Function 7. Change R21738/R21801 for Auto detect and change PCIE/SATA re-driver IC EQ0/EQ1 setting for EA fail 8. Add R67364/R67365 for power detect 9.Delete PWM IC of FAN LED 10.Delete Macro Key LED Conn
ZGL REV:C	5/2	1. Change 0 ohm resistor to shortpad 2. Change Q7945 & Q7821 value to "NVSR@" for NVSR function 3. Stuff R67380 & un-stuff D13095 for throtting issue 4. Add R67381 & reserve R67396 for detect issue, stuff R20915/R20917 for EA test fail 5. Change series resistor to 6.2 ohm for HDMI test 6. Add R67397 & reserve R67382 for monitor detect issue in type-c conn 7. Add "I2C1_XXX" & "2ND_MBXX" signals in TI solution of type-c conn 8. Add ESD jumper in USB port for Acer request 9. Change C94925 / C94929 to 0603 size, change R67206 / R67207 to 33 ohm for Realtek request and add U13161 for AMP vendor request 10. Modify REXT / EQ setting in left-side SSD conn 11. Delete "SIO_EXT_SMI#" signal for un-use 12. Modify R382 / R20887 to 100K ohm fot leakage issue 13. Add U13159 & related circuit for PWM IC leakage issue in LED side 14. Change R67023 to 374 ohm for LED brightness design 15. Add U13158 & related circuits to support keyboard wakeup
ZGL REV:D	6/5	1. Change 0 ohm resistor to shortpad 2. Keep Q34 in main source:PJX138K for HDMI HDCP issue 3. Change R67206 / R67207 to 47 ohm, stuff R67263 & un-stuff R67262, un-stuff C94947 & change R21454 to shortpad for AUDIO BOBO noise 4.Change R67023 to 931 ohm for LED brightness design

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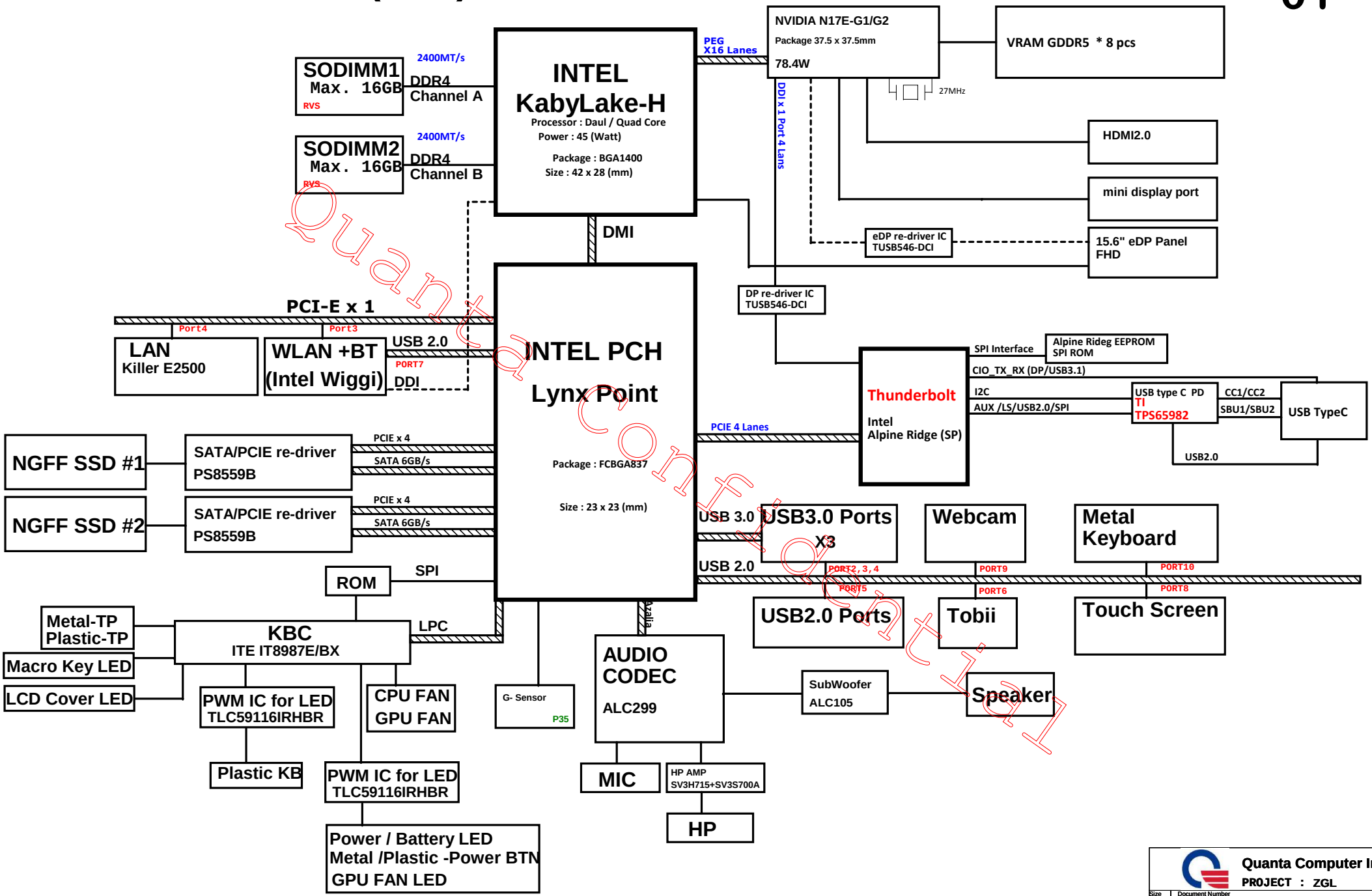
Falcon(ZGL) KBL-H +1060MAX P SYSTEM DIAGRAM

01



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Size	Document Number	Rev
	BLOCK DIAGRAM	3A

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H_PECI (50ohm)
Route on microstrip only
Spacing > 18 mils
Trace Length: 15 inch

{11} PCH_PECI — R563 13_1%_4 — {43} EC_PECI
C802 *47p/25V_2 — EC_PECI

Host CLK:
Trace length < 11000 MILS
Trace spacing = 15 ,20 MILS, Impendence 85 ohm

{11} CLK_CPU_BCLKP → BCLKP (B31)
{11} CLK_CPU_BCLKN → BCLKN (A32)
{11} CPU_PCI_BCLKP → PCI_BCLKP (D35)
{11} CPU_PCI_BCLKN → PCI_BCLKN (C36)
{11} CLK_DPLL_NSCCLKP → CLK24P (E31)
{11} CLK_DPLL_NSCCLKN → CLK24N (D31)

U41E SKYLAKE_HALO BGA1440

+VCCIO — R566 1K_1%_4 — H_PROHOT# — C96031 0.1u/10V_2
{43,53,57} H_PROHOT# — H_PROHOT# — R22148 499_1%_2 — H_PROCHOT#_CPU (BR30) — PROCHOT#
C807 47p/25V_2

PROCHOT# (50ohm)
Trace Length <11 inches

H_CPU_SVIDALRT# (BH31) — VIDALERT#
VR_SVID_CLK_R (BH32) — VIDSCK
H_CPU_SVIDDAT (BH29) — VIDSOUT
DDR_VTT_CNTL — BT13 — DDR_VTT_CNTL

CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

{11} CPU_PLTRST#R — R542 *750_1%_2 — R541 *1.5K_1%_2
{12,18,32,39,41,42,43,47,48} PLTRST#
{11} H_PM_DOWN — R559 20_1%_2

PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches

VCCST_PWRGD — H13 — VCCST_PWRGD
{10} PROCPWRGD — R560 *10K_1%_2 — BT31 — PROCPWRGD
{11} PM_SYNC — BP35 — RESET#
H_PM_DOWN_R (BM34) — PM_SYNC
EC_PECI (BP31) — PM_DOWN
PM_THRMTRIP# (BT34) — PECI
J31 — THERMTRIP#

{13} SKTOCC_N_R — R556 *Short_0402 — BR33 — SKTOCC_N
+1V_SUS — R181 *0_5%_4 — BN1 — SKTOCC#
+1V_SUS — R180 *100K_1%_4 — BM30 — PROC_SELECT#
+1V_SUS — R571 49.9_1%_2 — CATERR# — CATERR#

CFG[0] BN25 — T9019
CFG[1] BN27 — T9020
CFG[2] BN26 — CFG2 {8}
CFG[3] BN28 — CFG3 {8}
CFG[4] BR20 — CFG4 {8}
CFG[5] BM20 — CFG5 {8}
CFG[6] BT20 — CFG6 {8}
CFG[7] BP20 — CFG7 {8}
CFG[8] BR23 — T9021
CFG[9] BR22 — T9022
CFG[10] BT23 — CFG10 {8}
CFG[11] BT22
CFG[12] BM19 — CFG12 {8}
CFG[13] BR19 — CFG13 {8}
CFG[14] BP19 — T9009
CFG[15] BT19 — T9010
CFG[17] BN23 — T9011
CFG[16] BP23 — T9012
CFG[19] BP22 — T9013
CFG[18] BN22 — T9014
BPM#[0] BR27 — T9015
BPM#[1] BT27 — T9016
BPM#[2] BM31 — T9017
BPM#[3] BT30 — T9018

PROC_TDO — BT28 XDP_TDO_CPU
PROC_TDI — BL32 XDP_TDI_CPU
PROC_TMS — BP28 XDP_TMS_CPU
PROC_TCK — BR28 XDP_TCK
PROC_TRST# — BP30 XDP_TRST# — XDP_TRST# {15}
PROC_PREQ# — BL30 XDP_PREQ# — XDP_PREQ# {15}
PROC_PRDY# — BP27 XDP_PRDY# — XDP_PRDY# {15}
CFG_RCOMP — BT25 CFG_RCOMP — R129 49.9_1%_2

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KBL_H_BGA1440P

XDP_TDO_CPU — R578 51_1%_2 — R20758 *Short_0402 — +VCCIO
XDP_TMS_CPU — R20753 *51_1%_2
XDP_TDI_CPU — R20754 *51_1%_2
XDP_PREQ# — R20755 *51_1%_2 — R20757 *0_5%_2 — +1V_SUS
XDP_TCK — R20756 51_1%_2
XDP_TRST# — R564 51_1%_2

CPU thermal trip

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches

+1V_SUS — R184 *100K_1%_4
{10,57} IMVP_PWRGD — Q20 DMG301NU-7
+1V_SUS — R20751 1K_1%_4 — R191 1K_1%_4
PM_THRMTRIP# — Q23 METR3904-G — SYS_SHDN# {43,54,60}
PM_THRMTRIP# {11,44}

CPU CORE SVID

Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.

CLOSE TO CPU

+1V_SUS — R538 56.2_1%_2 — C755 0.1u/10V_2
H_CPU_SVIDALRT# — R545 220_1%_2 — VR_SVID_ALERT# {57}

CLOSE TO VR
PULL UP IS IN THE VR MODULE

+1V_SUS — R539 *54.9_1%_2 — C85 0.1u/10V_2
VR_SVID_CLK_R — R540 *Short_0402 — VR_SVID_CLK {57}

CLOSE TO CPU
PLACE THE PU RESISTORS

+1V_SUS — R544 100_1%_2 — C96159 0.1u/10V_2
H_CPU_SVIDDAT — R543 *Short_0402 — VR_SVID_DATA {57}

VCCST PWRGD

+3V_DEEP_SUS — C812 *0.1u/10V_2
{10,43} SUSB# — U53 *NL17SZ08DFT2G — VCCST_PWRGD_EN_L
HWPG — R202 *0_5%_4 — VCCST_PWRGD_EN
{10,43} PCH_PWROK — R204 *0_5%_4
R205 10K_1%_2
VCCST_PG

U13064 *74AUP1G07GW
NC VCC A GND Y
+3V_DEEP_SUS — C420 *0.1u/10V_2
+1V_SUS — R178 1K_1%_4
+VCCIO — R20752 *1K_1%_4
VCCST_PWRGD_R — R179 60.4_1%_4 — VCCST_PWRGD
C417 0.1u/10V_2
D13069 RB500V-40

Co-lay for ODT : From Intel MOW, ODT directly connection to CPU

+1.2VSUS — R21410 *47K_1%_4 — R21411 *47K_1%_4 — +3V_DEEP_SUS — R21412 *47K_1%_4
DDR_VTT_CNTL — Q7844 *LTC044EUBFS8TL — DDR_VTTT_PG_CTRL {56}

Power Side : MAINON Control to DDRVTT

+VCCIO — R21170 4.99K_1%_4
+5V_S5 — R21165 1K_1%_4
+3V_DEEP_SUS — R21164 10K_1%_2
+1.0V_PWRGD_G2 — Q7840 2N7002KTB — R21171 100K_1%_4
+1.0V_PWRGD_G1 — Q7842 METR3904-G
C94818 *0.1u/10V_2 — R21173 *100K_1%_4
HWPG_R — R21166 *Short_0402 — VCCST_PG
R67199 *0_5%_4 — HWPG — HWPG {43}

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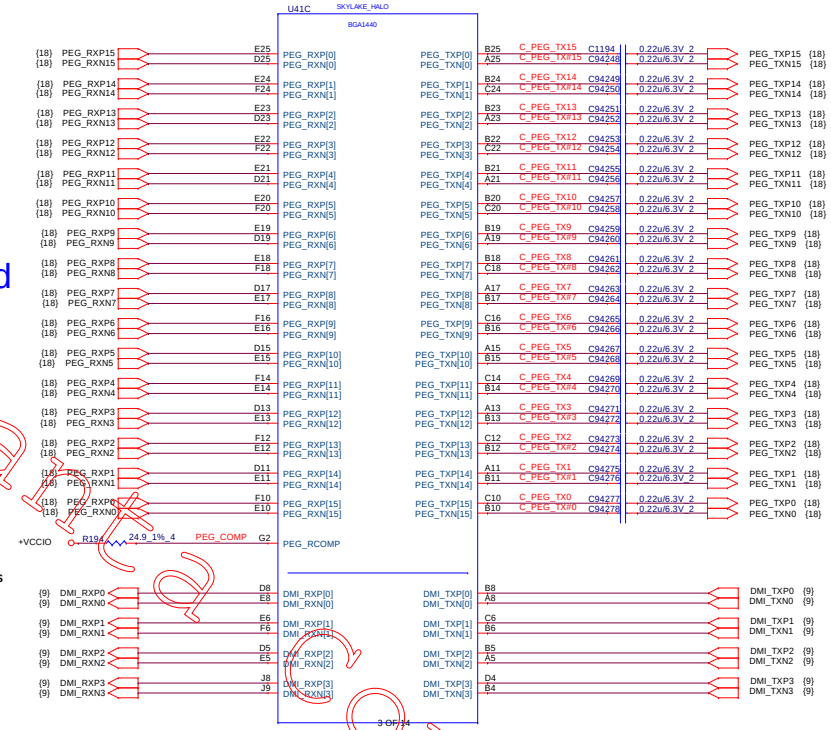
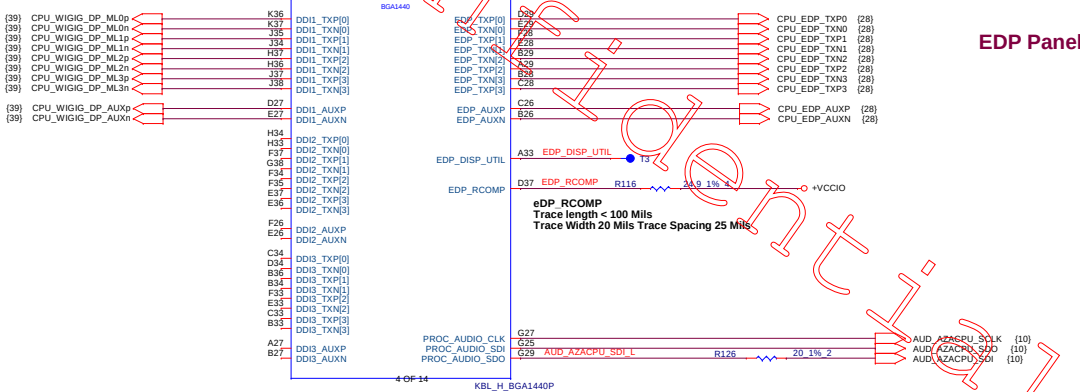
dGPU PEG*16
Lane Reversed



dGPU PEG*16
Lane Reversed

DMI



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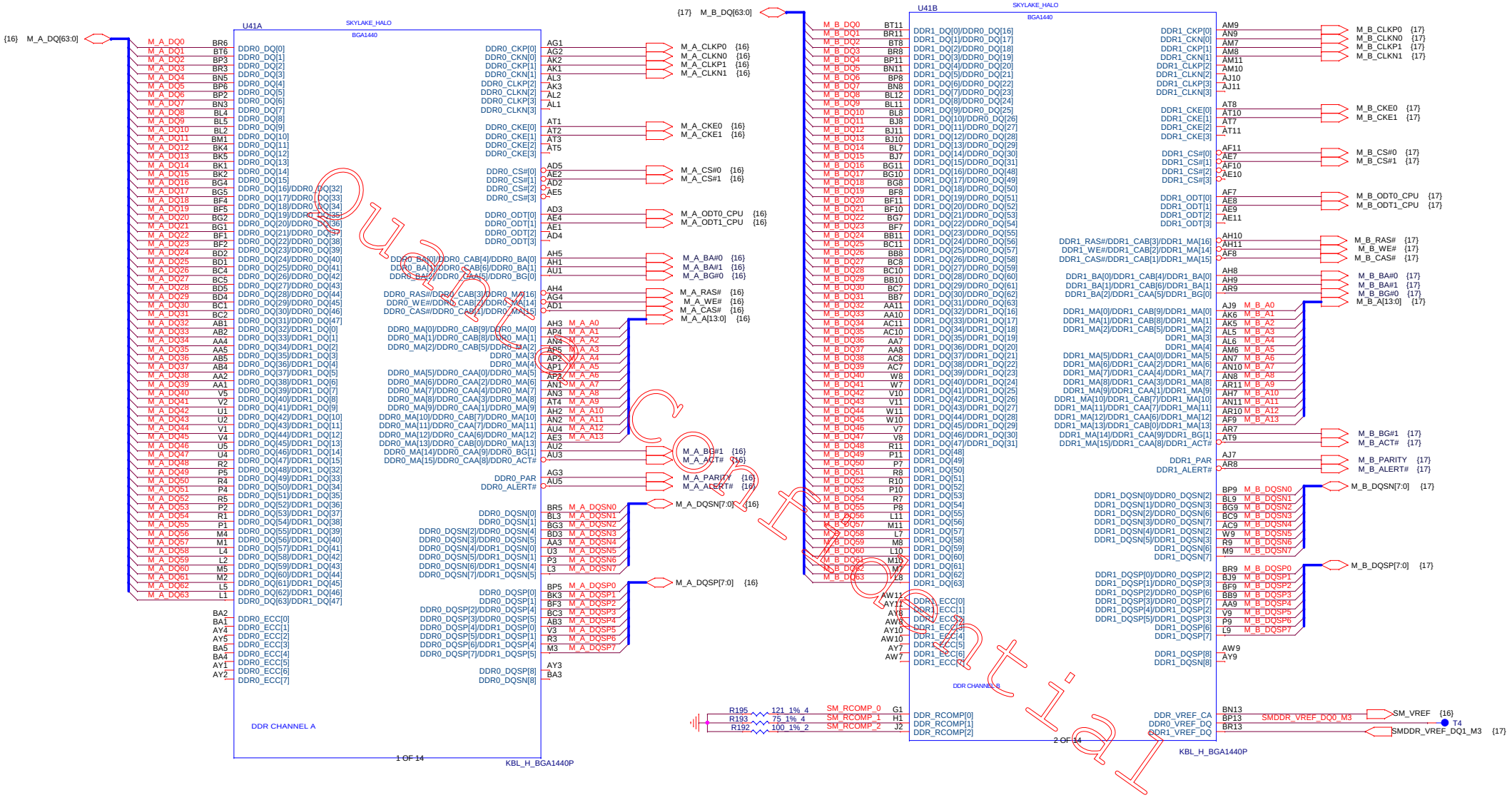
PROJECT : ZGL		
Size	Document Number: KBL 2/7 (DMI/EDP/PEG)	Rev: 3A
Date: Friday, June 23, 2017	Sheet 3 of 68	



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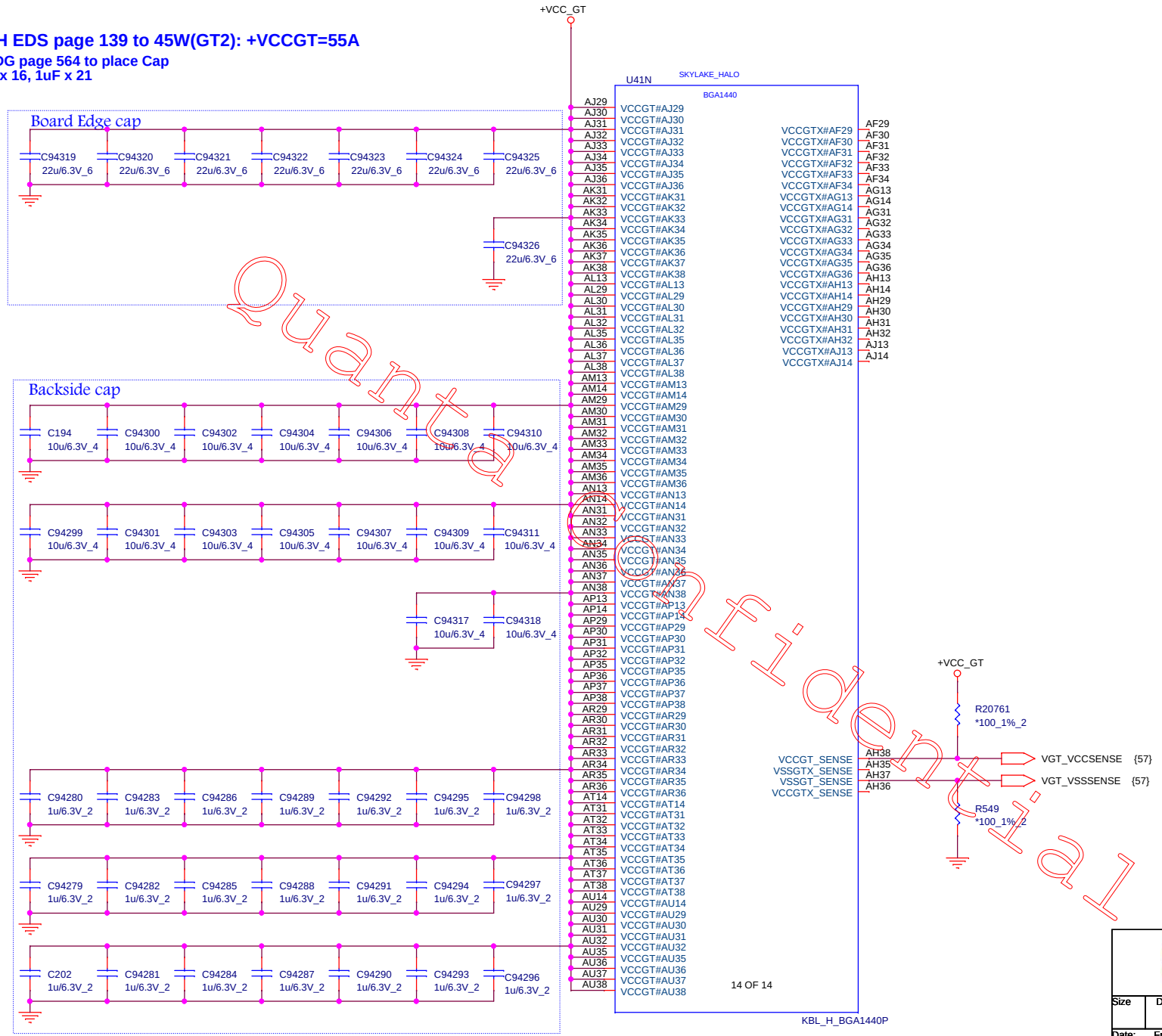
PROJECT : ZGL		
Size	Document Number: KBL 3/7 (DDR3 I/F)	Rev: 3A
Date: Friday, June 23, 2017	Sheet 4 of 68	

Follow KBL H EDS page 139 to 45W(GT2): +VCCGT=55A

Follow KBL H DG page 564 to place Cap
22uF x 8, 10uF x 16, 1uF x 21

05



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PROJECT : ZGL		
Size	Document Number	Rev
	KBL 4/7 (POWER)	3A
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Follow KBL H EDS page 141 to 45W(GT2): VCCSA=11.1A

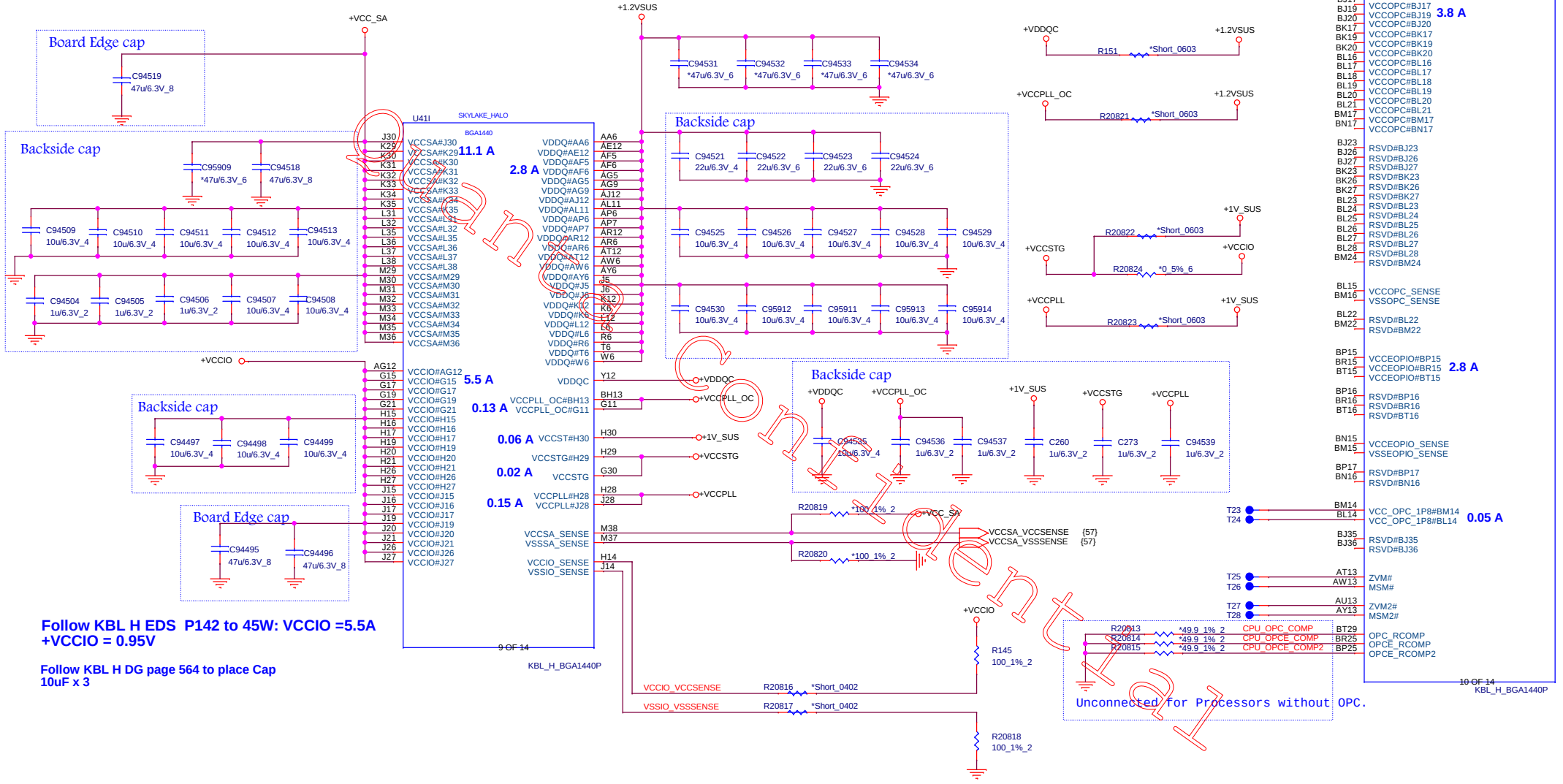
Follow KBL H DG page 564 to place Cap
47uF x 2, 10uF x 7, 1uF x3

Follow KBL H EDS page 141 45W: VDDQ=2.8A

Follow KBL H DG page 564 to place Cap
22uF x 4, 10uF x 10

Follow KBL H EDS P142 to 45W: VCCIO =5.5A
+VCCIO = 0.95V

Follow KBL H DG page 564 to place Cap
10uF x 3



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PROJECT : ZGL
Size | Document Number: KBL 5/7 (POWER&GND) | Rev 3A
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Follow KBL H EDS page 137 to 45W(GT2): VCC_CORE=68A

Follow KBL H DG page 564 to place Cap
47uF x 4, 22uF x 8, 10uF x 28, 1uF x63

Board Edge cap

C94423 47u/6.3V_8 C94424 47u/6.3V_8 C94425 47u/6.3V_8 C94426 47u/6.3V_8

Backside cap

C94411 C94412 C94413 C94414 C94415 C94416 22u/6.3V_6

C94417 C94418 22u/6.3V_6

C94398 C94395 C94396 C94397 C94402 C94399 C94400 C94401 10u/6.3V_4

C94406 C94403 C94404 C94405 C94410 C94407 C94408 C94409 10u/6.3V_4

C94394 C94391 C94392 C94393 C94390 C94387 C94388 C94389 10u/6.3V_4

C767 C94384 C94385 C94386 10u/6.3V_4

+VCC_CORE

U41G SKYLAKE_HALO BGA1440

AA13	VCC#AA13	VCC#V32	V32
AA31	VCC#AA31	VCC#V33	V33
AA32	VCC#AA32	VCC#V34	V34
AA33	VCC#AA33	VCC#V35	V35
AA34	VCC#AA34	VCC#V36	V36
AA35	VCC#AA35	VCC#V37	V37
AA36	VCC#AA36	VCC#V38	V38
AA37	VCC#AA37	VCC#W13	W13
AA38	VCC#AA38	VCC#W14	W14
AB29	VCC#AB29	VCC#W29	W29
AB30	VCC#AB30	VCC#W30	W30
AB31	VCC#AB31	VCC#W31	W31
AB32	VCC#AB32	VCC#W32	W32
AB35	VCC#AB35	VCC#W35	W35
AB36	VCC#AB36	VCC#W36	W36
AB37	VCC#AB37	VCC#W37	W37
AB38	VCC#AB38	VCC#W38	W38
AC13	VCC#AC13	VCC#Y29	Y29
AC14	VCC#AC14	VCC#Y30	Y30
AC29	VCC#AC29	VCC#Y31	Y31
AC30	VCC#AC30	VCC#Y32	Y32
AC31	VCC#AC31	VCC#Y33	Y33
AC32	VCC#AC32	VCC#Y34	Y34
AC33	VCC#AC33	VCC#Y35	Y35
AC34	VCC#AC34	VCC#Y36	Y36
AC35	VCC#AC35	VCC#L14	L14
AC36	VCC#AC36	VCC#P29	P29
AD13	VCC#AD13	VCC#P30	P30
AD14	VCC#AD14	VCC#P31	P31
AD31	VCC#AD31	VCC#P32	P32
AD32	VCC#AD32	VCC#P33	P33
AD33	VCC#AD33	VCC#P34	P34
AD34	VCC#AD34	VCC#P35	P35
AD35	VCC#AD35	VCC#P36	P36
AD36	VCC#AD36	VCC#R13	R13
AD37	VCC#AD37	VCC#R31	R31
AD38	VCC#AD38	VCC#R32	R32
AE13	VCC#AD39	VCC#R33	R33
AE14	VCC#AE13	VCC#R34	R34
AE30	VCC#AE14	VCC#R35	R35
AE31	VCC#AE30	VCC#R36	R36
AE32	VCC#AE31	VCC#R37	R37
AE35	VCC#AE32	VCC#R38	R38
AE36	VCC#AE35	VCC#T29	T29
AE37	VCC#AE36	VCC#T30	T30
AE38	VCC#AE37	VCC#T31	T31
AF35	VCC#AE38	VCC#T32	T32
AF36	VCC#AF35	VCC#T35	T35
AF37	VCC#AF36	VCC#T36	T36
AF38	VCC#AF37	VCC#T37	T37
K13	VCC#AF38	VCC#T38	T38
K14	VCC#K13	VCC#U29	U29
L13	VCC#K14	VCC#U30	U30
N13	VCC#L13	VCC#U31	U31
N14	VCC#N13	VCC#U32	U32
N30	VCC#N14	VCC#U33	U33
N31	VCC#N30	VCC#U34	U34
N32	VCC#N31	VCC#U35	U35
N35	VCC#N32	VCC#U36	U36
N36	VCC#N35	VCC#V13	V13
N37	VCC#N36	VCC#V14	V14
N38	VCC#N37	VCC#V31	V31
P13	VCC#N38	VCC#P14	P14
	VCC#P13		

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KBL_H_BGA1440P

Backside cap

C94486 C94490 C94493 C94492 C94494 C94487 C94489 C94488 C94491 1u/6.3V_2

C94477 C94481 C94484 C94483 C94485 C94478 C94480 C94479 C94482 1u/6.3V_2

C94468 C94472 C94475 C94474 C94476 C94469 C94471 C94470 C94473 1u/6.3V_2

C94459 C94463 C94466 C94465 C94467 C94460 C94462 C94461 C94464 1u/6.3V_2

C94451 C94455 C94456 C94457 C94458 C94450 C94452 C94453 C94454 1u/6.3V_2

C94442 C94446 C94447 C94448 C94449 C94441 C94443 C94444 C94445 1u/6.3V_2

C94432 C94433 C94434 C94435 C94436 C94437 C94438 C94439 C94440 1u/6.3V_2

Sense resistor should be placed within 2 inches (50.8 mm) of the processor socket

Trace Impendence 50 ohm

R20812 *100 1% 2 +VCC_CORE

VCC_SENSE AG37 VCCSENSE VCCSENSE {57}

VSS_SENSE AG38 VSSSENSE VSSSENSE {57}

R547 *100 1% 2

VCCSENSE R552 *49.9 1% 2 VSSSENSE

+VCC_GT

U41H SKYLAKE_HALO BGA1440

BG34	VCCGT#BG34	VCCGT#AV29	AV29
BG35	VCCGT#BG35	VCCGT#AV30	AV30
BG36	VCCGT#BG36	VCCGT#AV31	AV31
BH33	VCCGT#BH33	VCCGT#AV32	AV32
BH34	VCCGT#BH34	VCCGT#AV33	AV33
BH35	VCCGT#BH35	VCCGT#AV34	AV34
BH36	VCCGT#BH36	VCCGT#AV35	AV35
BH37	VCCGT#BH37	VCCGT#AV36	AV36
BH38	VCCGT#BH38	VCCGT#AW14	AW14
BJ37	VCCGT#BJ37	VCCGT#AW31	AW31
BJ38	VCCGT#BJ38	VCCGT#AW32	AW32
BL36	VCCGT#BL36	VCCGT#AW33	AW33
BL37	VCCGT#BL37	VCCGT#AW34	AW34
BM36	VCCGT#BM36	VCCGT#AW35	AW35
BM37	VCCGT#BM37	VCCGT#AW36	AW36
BN36	VCCGT#BN36	VCCGT#AW37	AW37
BN37	VCCGT#BN37	VCCGT#AW38	AW38
BN38	VCCGT#BN38	VCCGT#AY29	AY29
BP37	VCCGT#BP37	VCCGT#AY30	AY30
BP38	VCCGT#BP38	VCCGT#AY31	AY31
BR37	VCCGT#BR37	VCCGT#AY32	AY32
BT37	VCCGT#BT37	VCCGT#AY35	AY35
BE38	VCCGT#BE38	VCCGT#AY36	AY36
BF13	VCCGT#BF13	VCCGT#AY37	AY37
BF14	VCCGT#BF14	VCCGT#AY38	AY38
BF29	VCCGT#BF29	VCCGT#BA13	BA13
BF30	VCCGT#BF30	VCCGT#BA14	BA14
BF31	VCCGT#BF31	VCCGT#BA29	BA29
BF32	VCCGT#BF32	VCCGT#BA30	BA30
BF35	VCCGT#BF35	VCCGT#BA31	BA31
BF36	VCCGT#BF36	VCCGT#BA32	BA32
BF37	VCCGT#BF37	VCCGT#BA33	BA33
BF38	VCCGT#BF38	VCCGT#BA34	BA34
BG29	VCCGT#BG29	VCCGT#BA35	BA35
BG30	VCCGT#BG30	VCCGT#BA36	BA36
BG31	VCCGT#BG31	VCCGT#BB13	BB13
BG32	VCCGT#BG32	VCCGT#BB14	BB14
BG33	VCCGT#BG33	VCCGT#BB31	BB31
BC36	VCCGT#BC36	VCCGT#BB32	BB32
BC37	VCCGT#BC37	VCCGT#BB33	BB33
BC38	VCCGT#BC38	VCCGT#BB34	BB34
BD13	VCCGT#BD13	VCCGT#BB35	BB35
BD14	VCCGT#BD14	VCCGT#BB36	BB36
BD29	VCCGT#BD29	VCCGT#BB37	BB37
BD30	VCCGT#BD30	VCCGT#BB38	BB38
BD31	VCCGT#BD31	VCCGT#BC29	BC29
BD32	VCCGT#BD32	VCCGT#BC30	BC30
BD33	VCCGT#BD33	VCCGT#BC31	BC31
BD34	VCCGT#BD34	VCCGT#BC32	BC32
BD35	VCCGT#BD35	VCCGT#BC35	BC35
BD36	VCCGT#BD36	VCCGT#BE33	BE33
BE31	VCCGT#BE31	VCCGT#BE34	BE34
BE32	VCCGT#BE32	VCCGT#BE35	BE35
BE37	VCCGT#BE37	VCCGT#BE36	BE36

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KBL_H_BGA1440P

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PROJECT : ZGL

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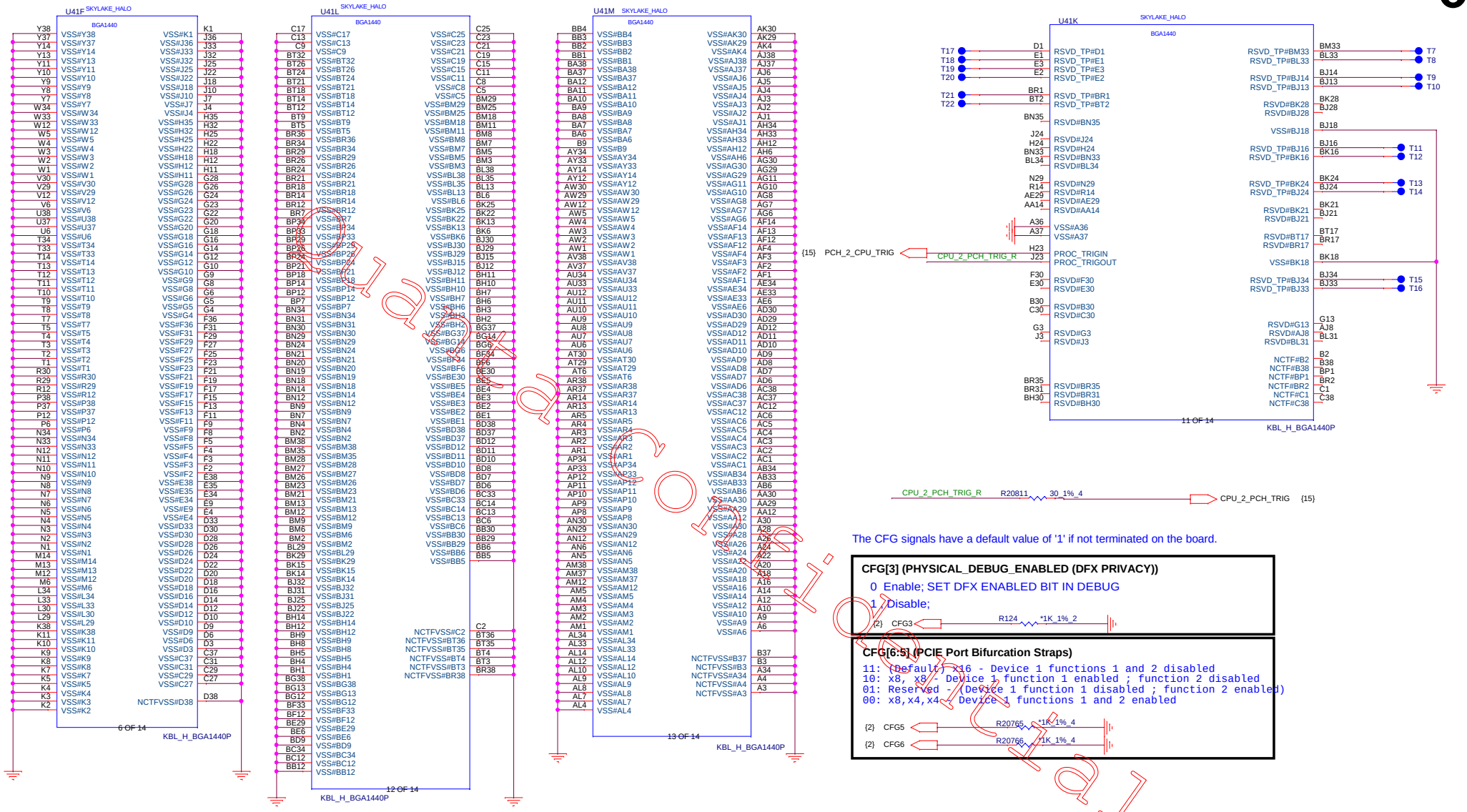

The CFG signals have a default value of '1' if not terminated on the board.

CFG[3] (PHYSICAL_DEBUG_ENABLED (DFX PRIVACY))

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 Disable;

{2} CFG3 R124 *1K_1%_2

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled

10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled

01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)

00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

{2} CFG5 R20765 *1K_1%_4

{2} CFG6 R20766 *1K_1%_4

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Training)	PEG train immediately following xxRESETB de assertion (Default)	PEG wait for BIOS training

{2} CFG2 R20767 1K_1%_4

{2} CFG4 R20768 OP@1K_1%_4

{2} CFG7 R67188 *1K_1%_4

{2} CFG10 R20764 *1K_1%_4

{2} CFG12 R20763 *1K_1%_4

{2} CFG13 R20762 *1K_1%_4

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	KBL 7/7 (POWER&GND)	3A

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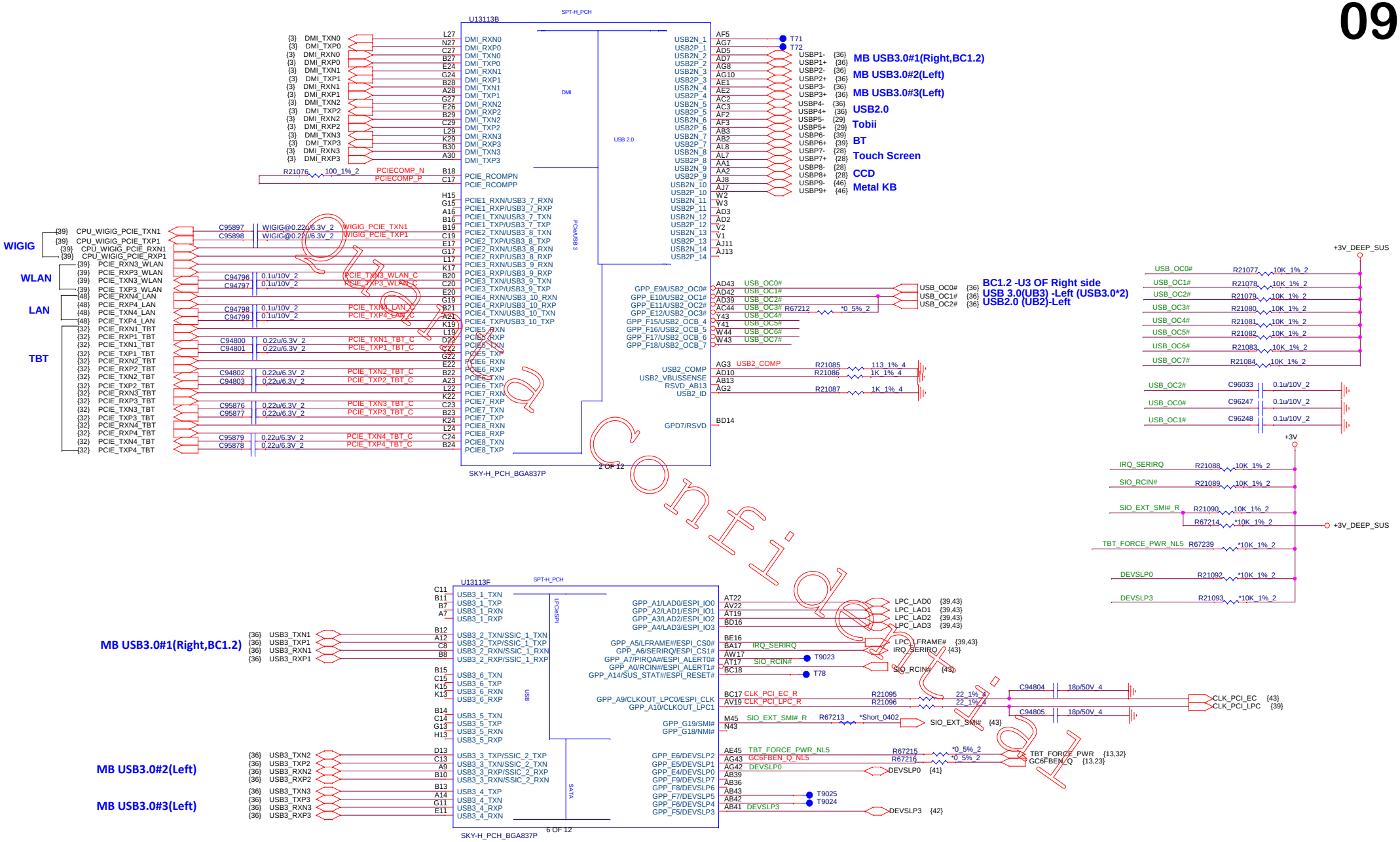

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	PCH 1/7 (DMI/USB/PCIE)	3A
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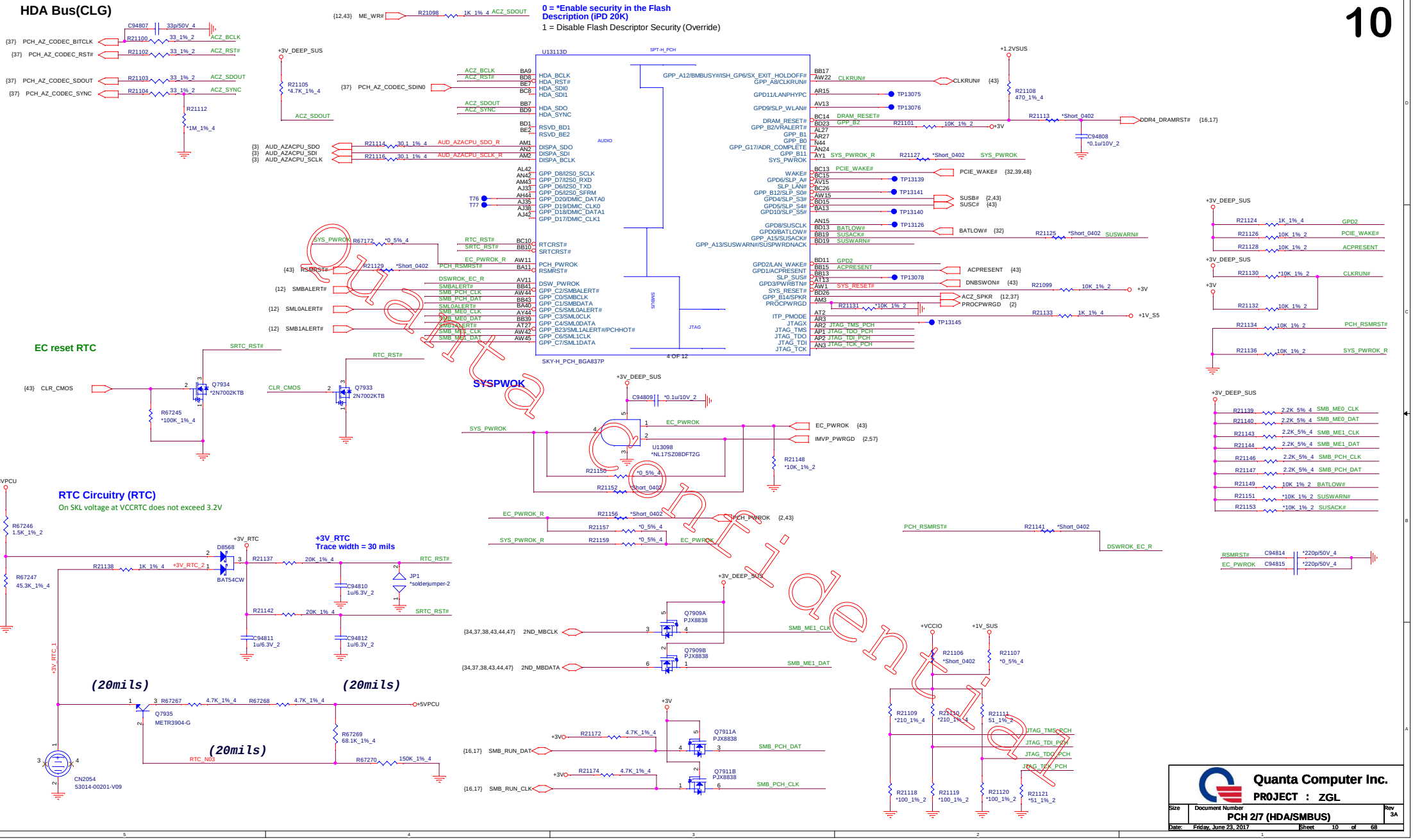
HDA Bus(CLG)



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Size	Document Number	Rev
	PCH 2/7 (HDA/SMBUS)	3A

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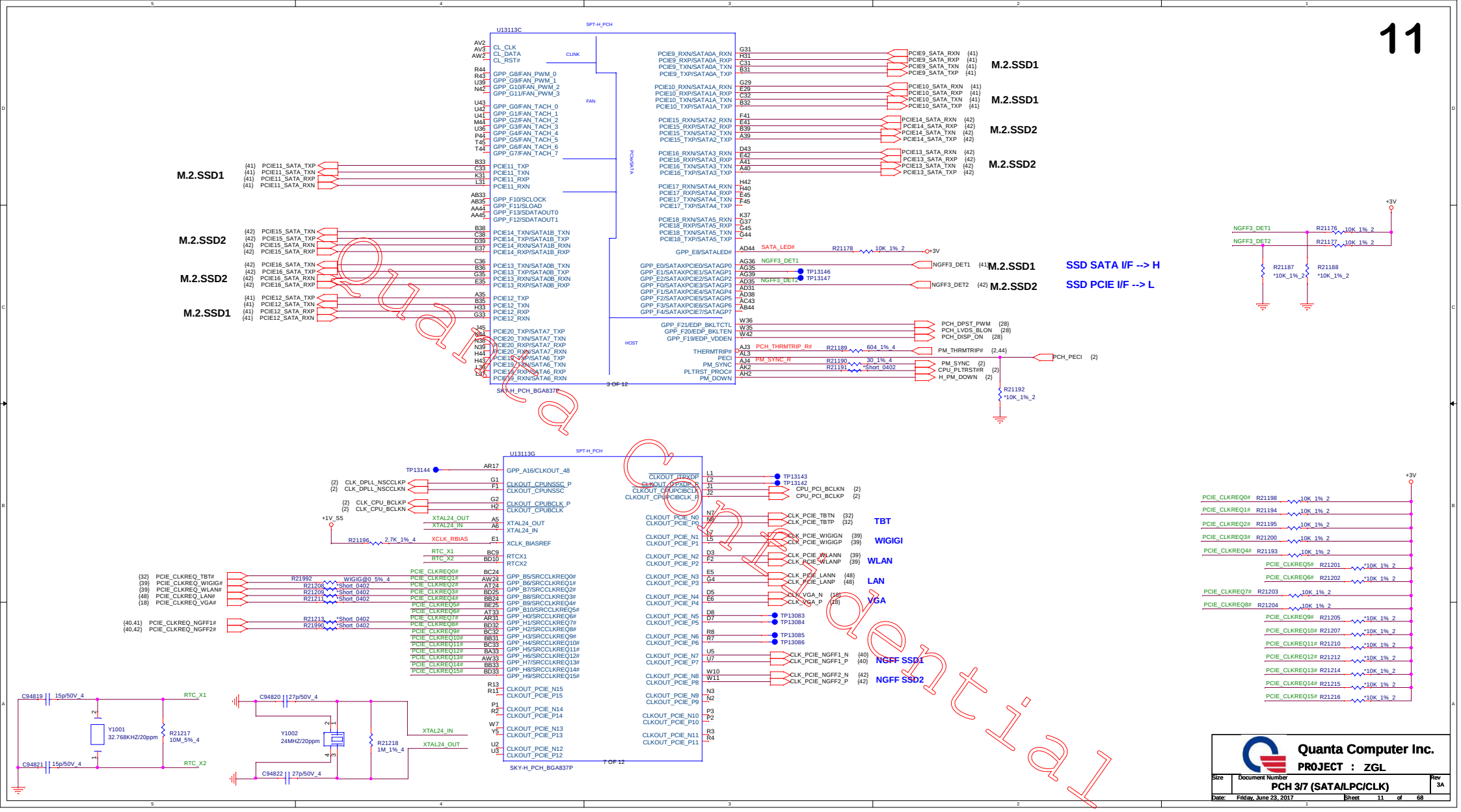

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Size	Document Number: PCH 3/7 (SATA/LPC/CLK)	Rev: 3A
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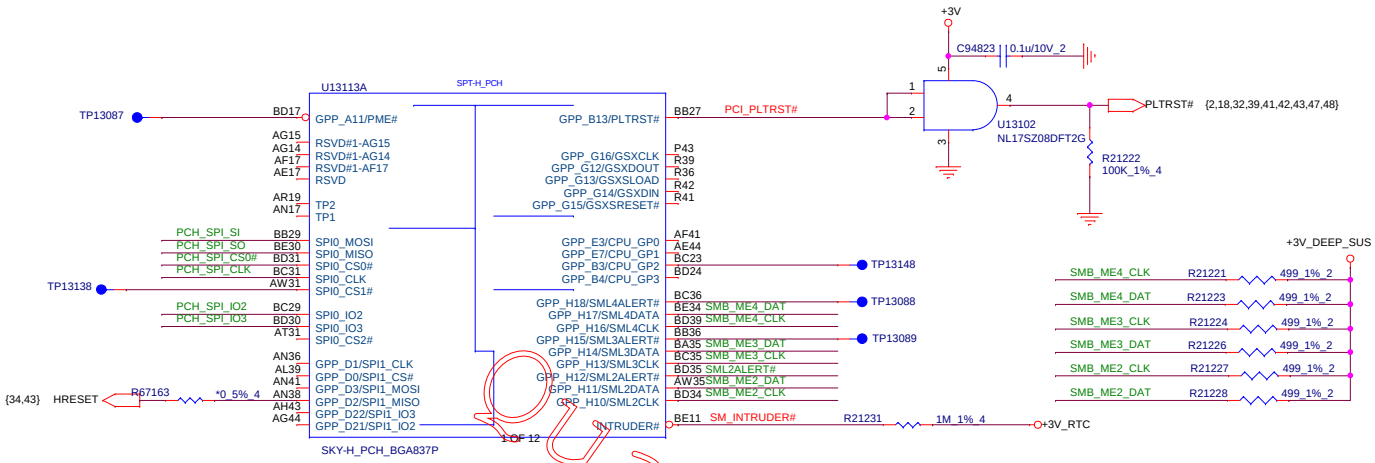

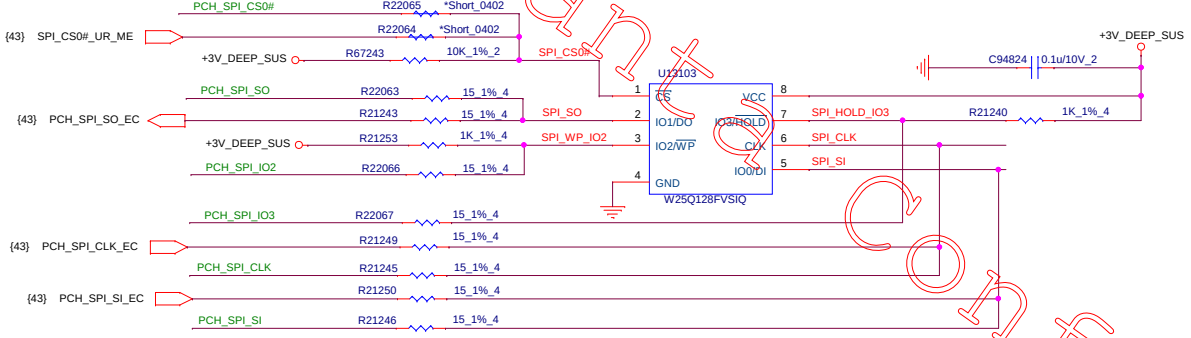

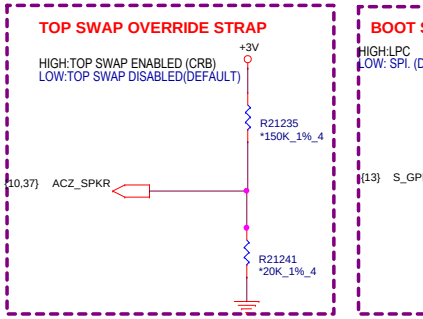

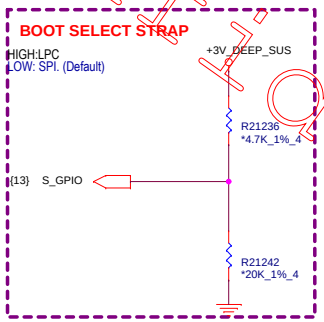

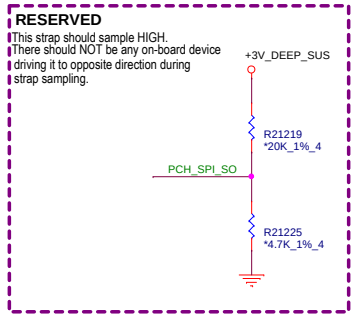

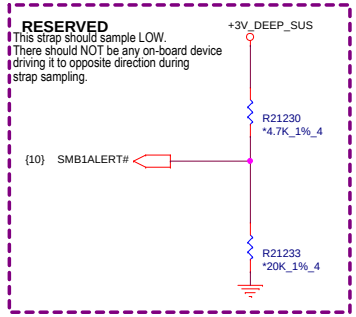

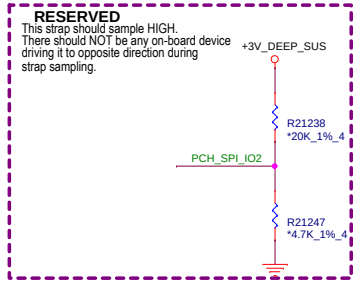

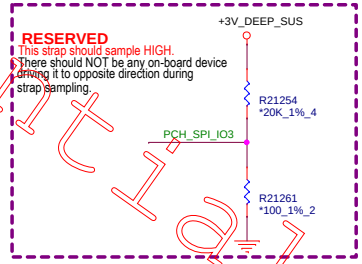

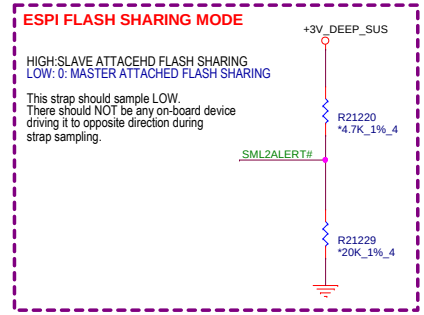

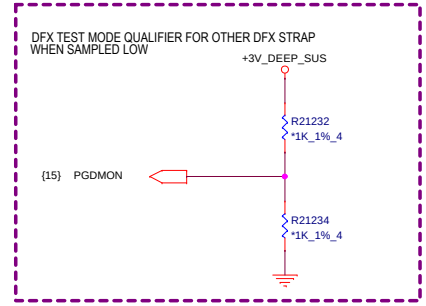

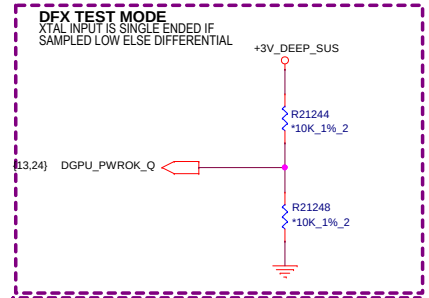

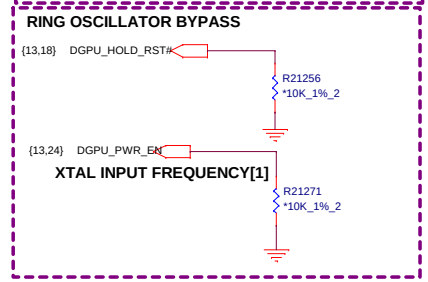

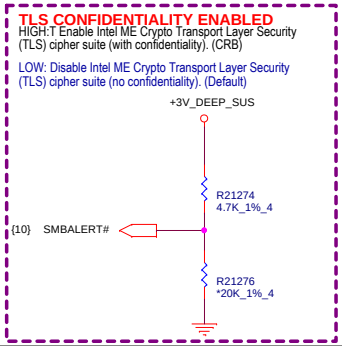

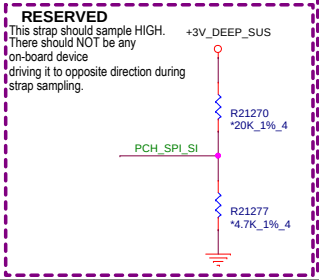

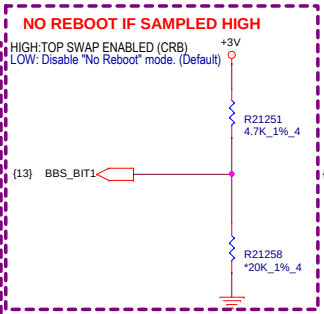

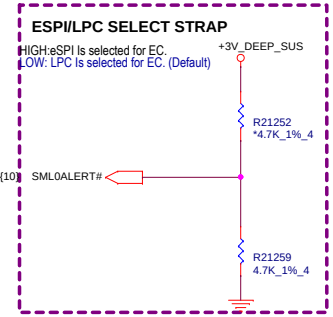

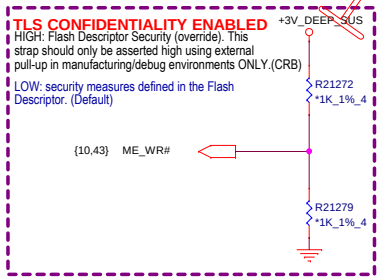

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	PCH 4/7 (GPIO/MISC)	3A
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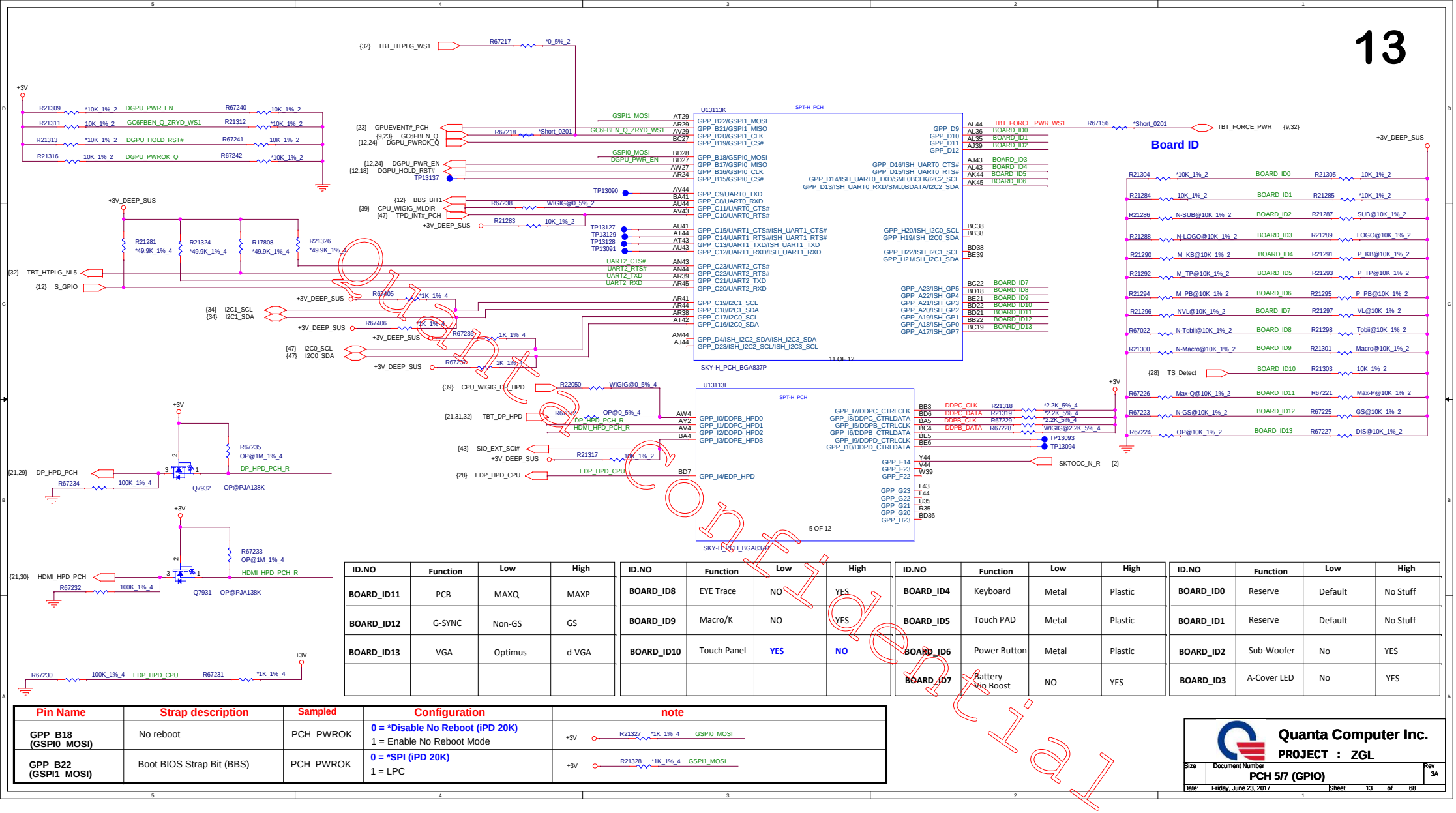

ID.NO	Function	Low	High
BOARD_ID11	PCB	MAXQ	MAXP
BOARD_ID12	G-SYNC	Non-GS	GS
BOARD_ID13	VGA	Optimus	d-VGA

ID.NO	Function	Low	High
BOARD_ID8	EYE Trace	NO	YES
BOARD_ID9	Macro/K	NO	YES
BOARD_ID10	Touch Panel	YES	NO

ID.NO	Function	Low	High
BOARD_ID4	Keyboard	Metal	Plastic
BOARD_ID5	Touch PAD	Metal	Plastic
BOARD_ID6	Power Button	Metal	Plastic
BOARD_ID7	Battery Vin Boost	NO	YES

ID.NO	Function	Low	High
BOARD_ID0	Reserve	Default	No Stuff
BOARD_ID1	Reserve	Default	No Stuff
BOARD_ID2	Sub-Woofer	No	YES
BOARD_ID3	A-Cover LED	No	YES

Pin Name	Strap description	Sampled	Configuration	note
GPP_B18 (GSPI0_MOSI)	No reboot	PCH_PWROK	0 = *Disable No Reboot (iPD 20K) 1 = Enable No Reboot Mode	+3V R21327 *1K_1%_4 GSPI0_MOSI
GPP_B22 (GSPI1_MOSI)	Boot BIOS Strap Bit (BBS)	PCH_PWROK	0 = *SPI (iPD 20K) 1 = LPC	+3V R21328 *1K_1%_4 GSPI1_MOSI

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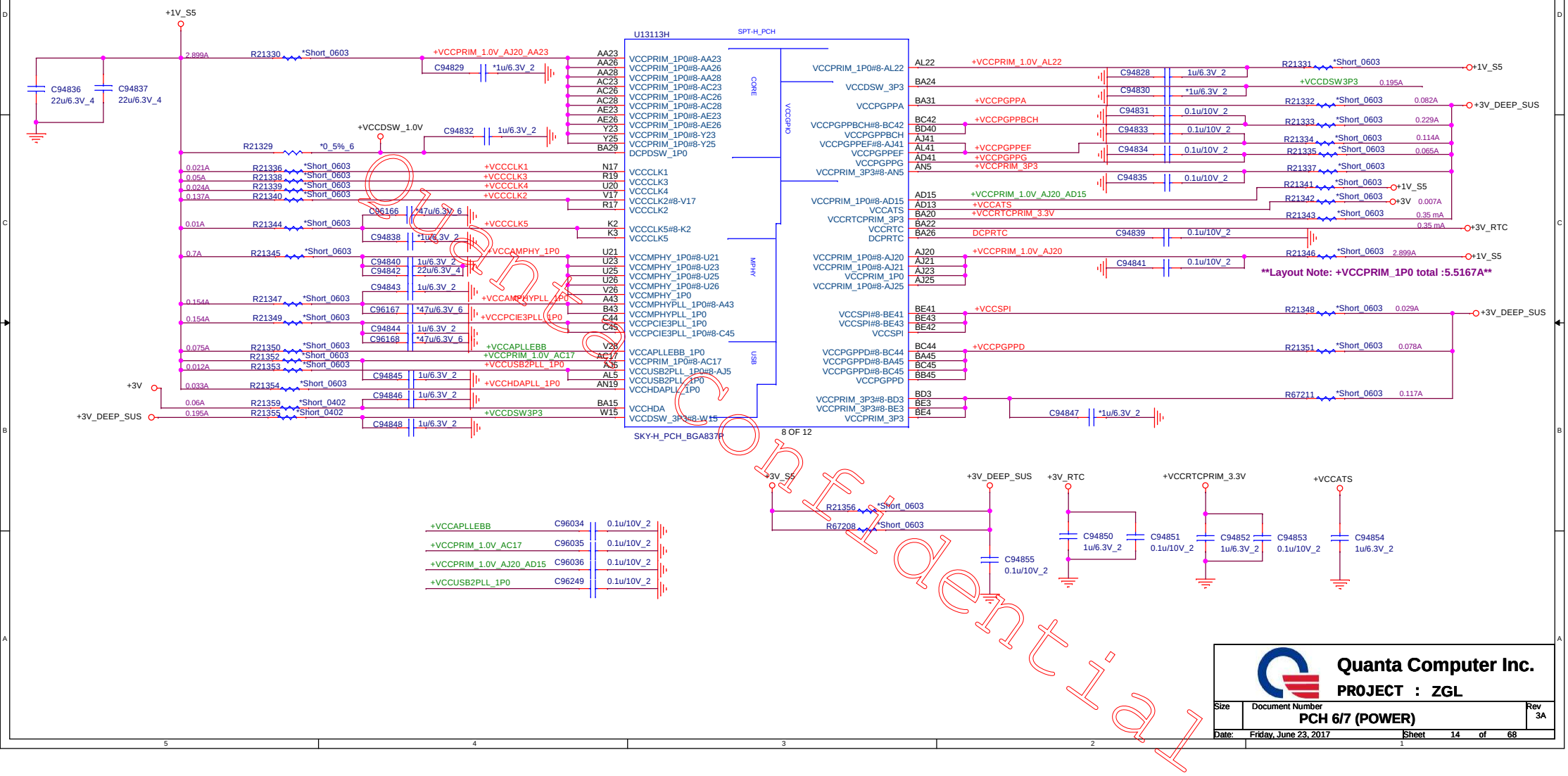
U13113H
SPT-H_PCH
SKY-H_PCH_BGA837P
8 OF 12
Layout Note: +VCCPRIM_1P0 total :5.5167A
+1V_S5
+3V_DEEP_SUS
+3V_RTC
+3V
+VCCDSW_1.0V
+VCCPRIM_1.0V_AJ20_AA23
+VCCPRIM_1.0V_AL22
+VCCPRIM_1.0V_AJ20_AD15
+VCCSPI
+VCCPGPPD
+VCCPGPPA
+VCCPGPPBCH
+VCCPGPPEF
+VCCPGPPG
+VCCRTCPRIM_3.3V
+VCCATS
+VCCCLK1
+VCCCLK3
+VCCCLK4
+VCCCLK2
+VCCCLK5
+VCCAMPHYPLL_1P0
+VCCPCIE3PLL_1P0
+VCCAPLLEBB
+VCCPRIM_1.0V_AC17
+VCCUSB2PLL_1P0
+VCCHDAPLL_1P0
+VCCDSW3P3
+VCCRTCPRIM_3.3V
+VCCATS
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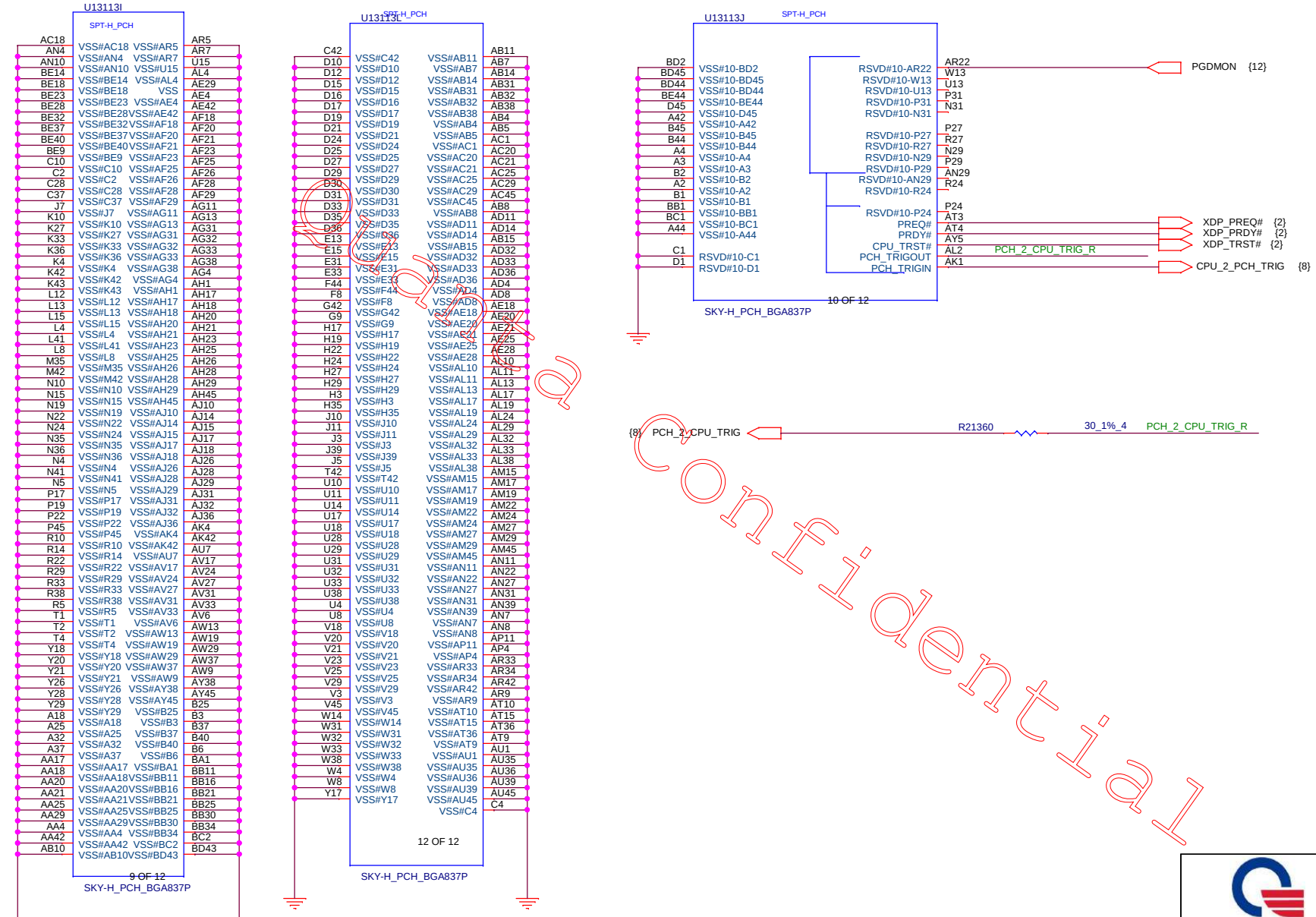

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Size	Document Number	Rev
	PCH 7/7 (GND)	3A
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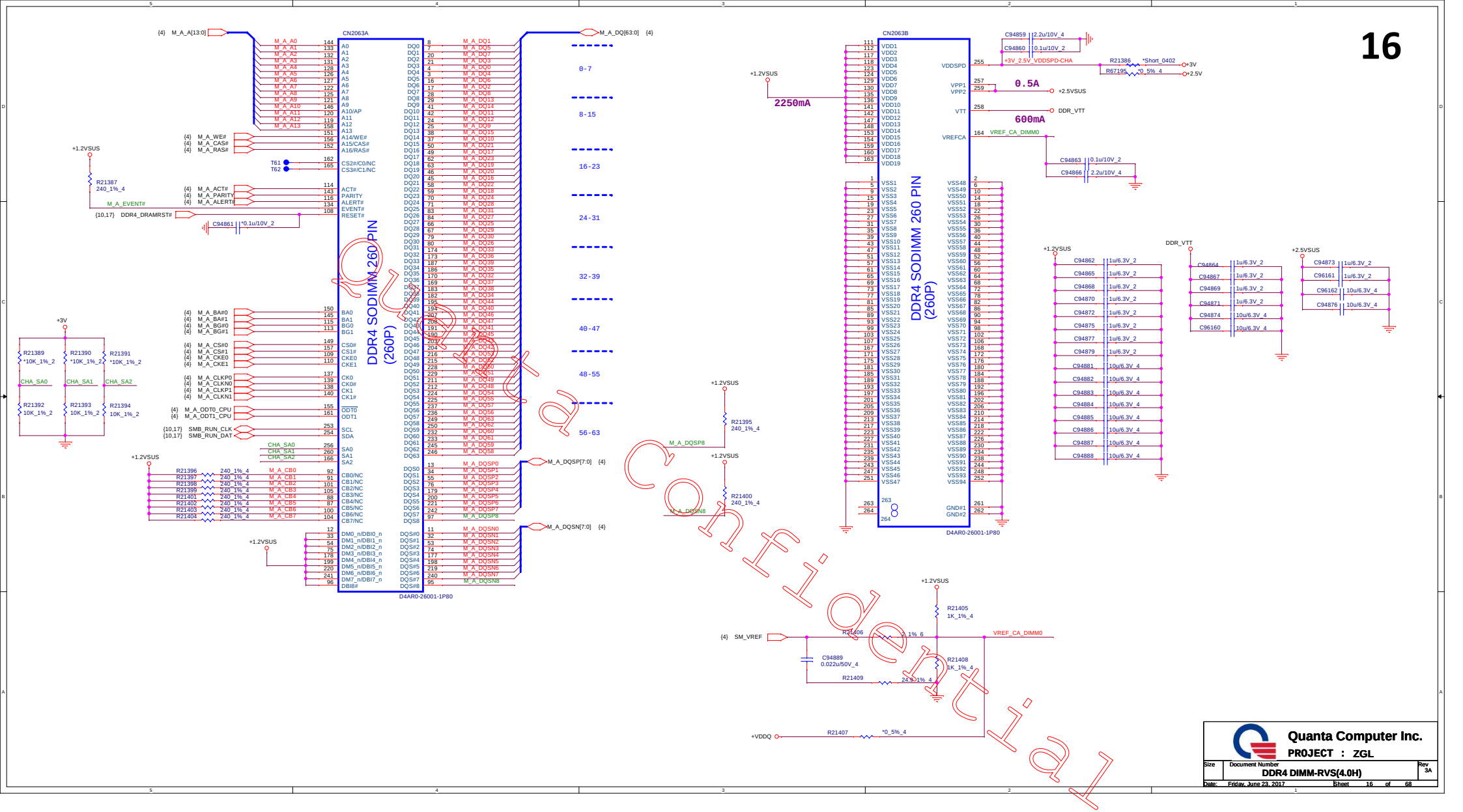

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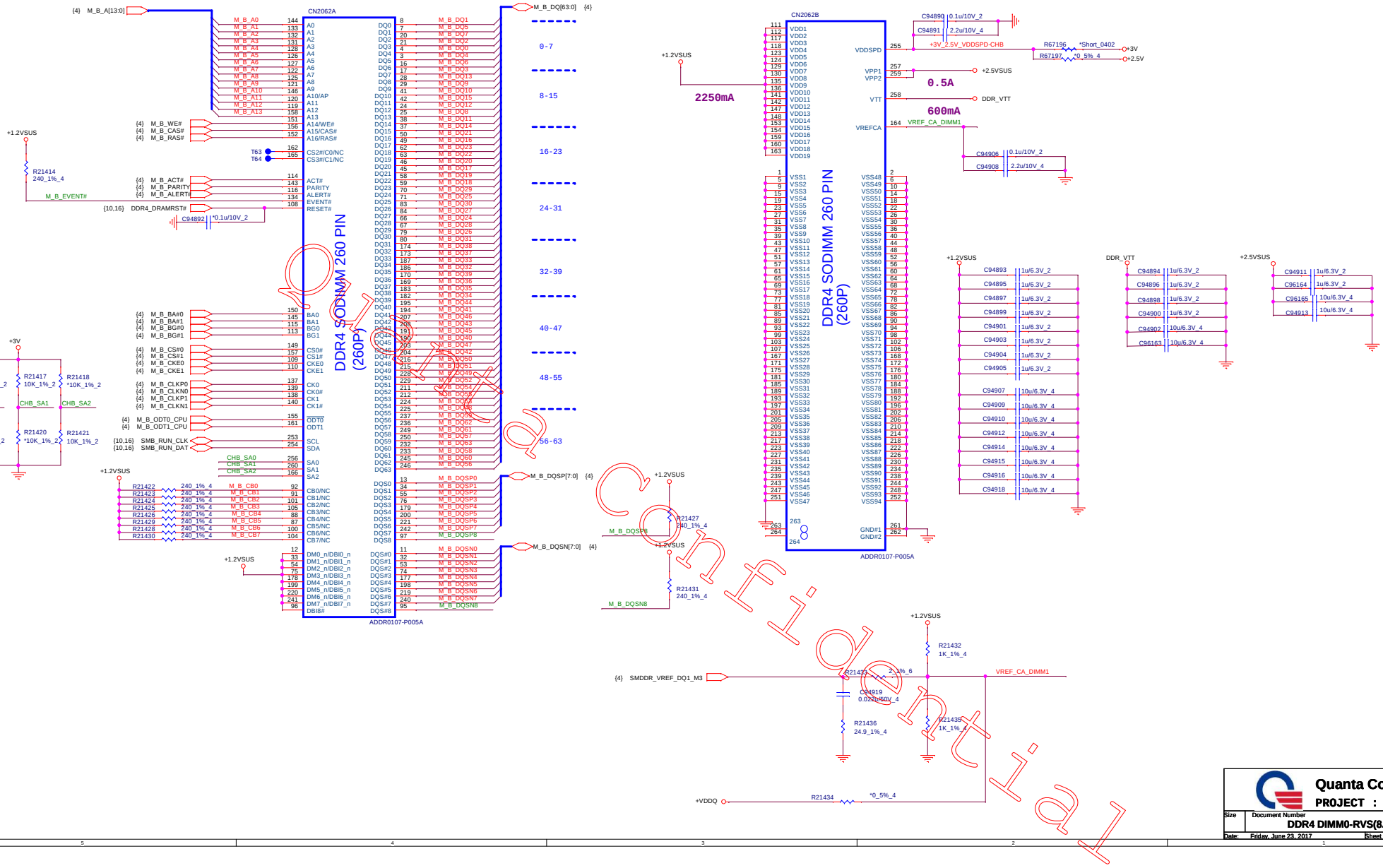
Size	Document Number		Rev
	DDR4 DIMM-RVS(4.0H)		3A
Date: Friday, June 23, 2017	Sheet 16 of 68		



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Size	Document Number: DDR4 DIMM0-RVS(8.0H)	Rev: 3A
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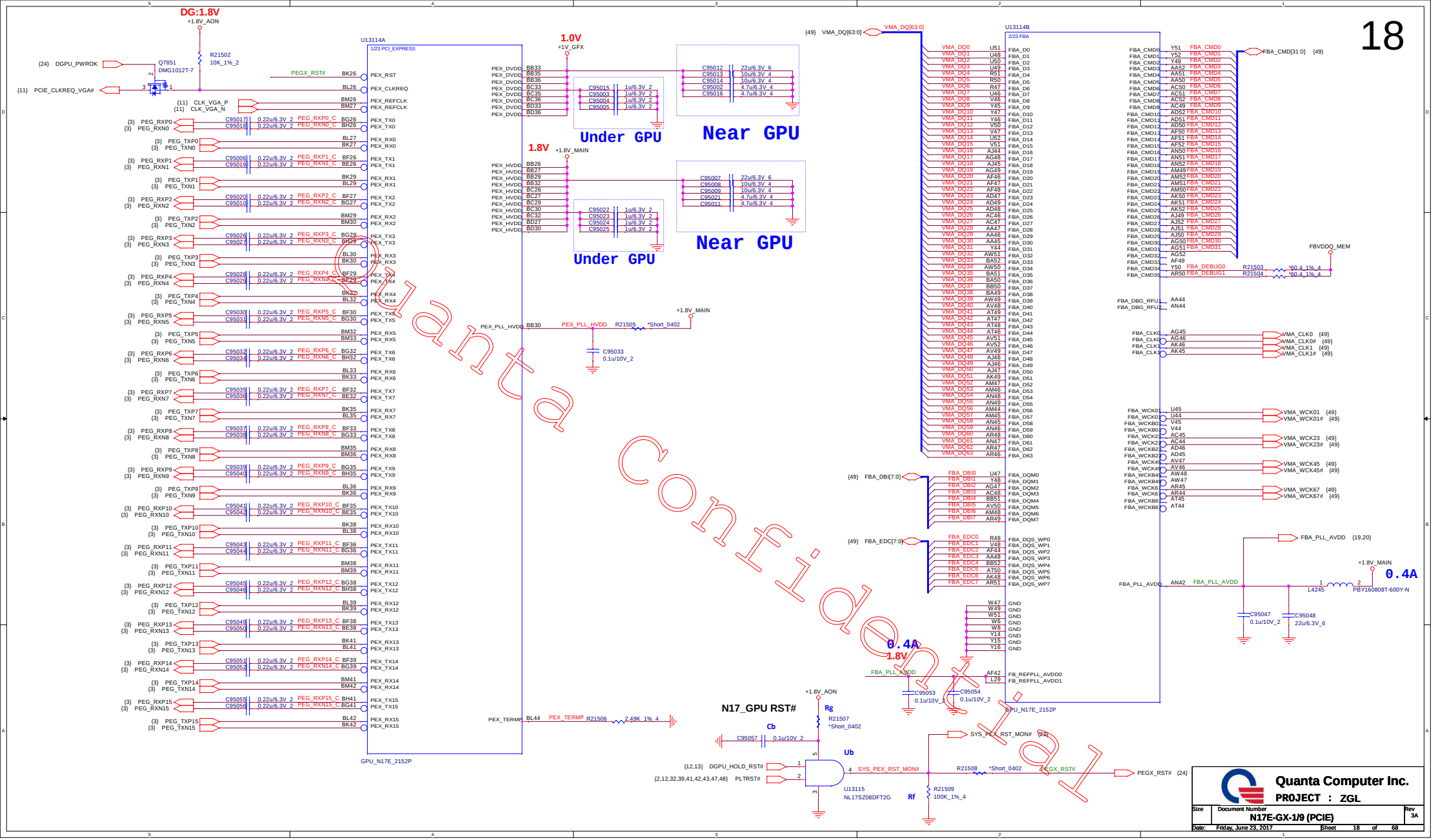

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Size	Document Number		Rev
	N17E-GX-1/9 (PCIE)		3A
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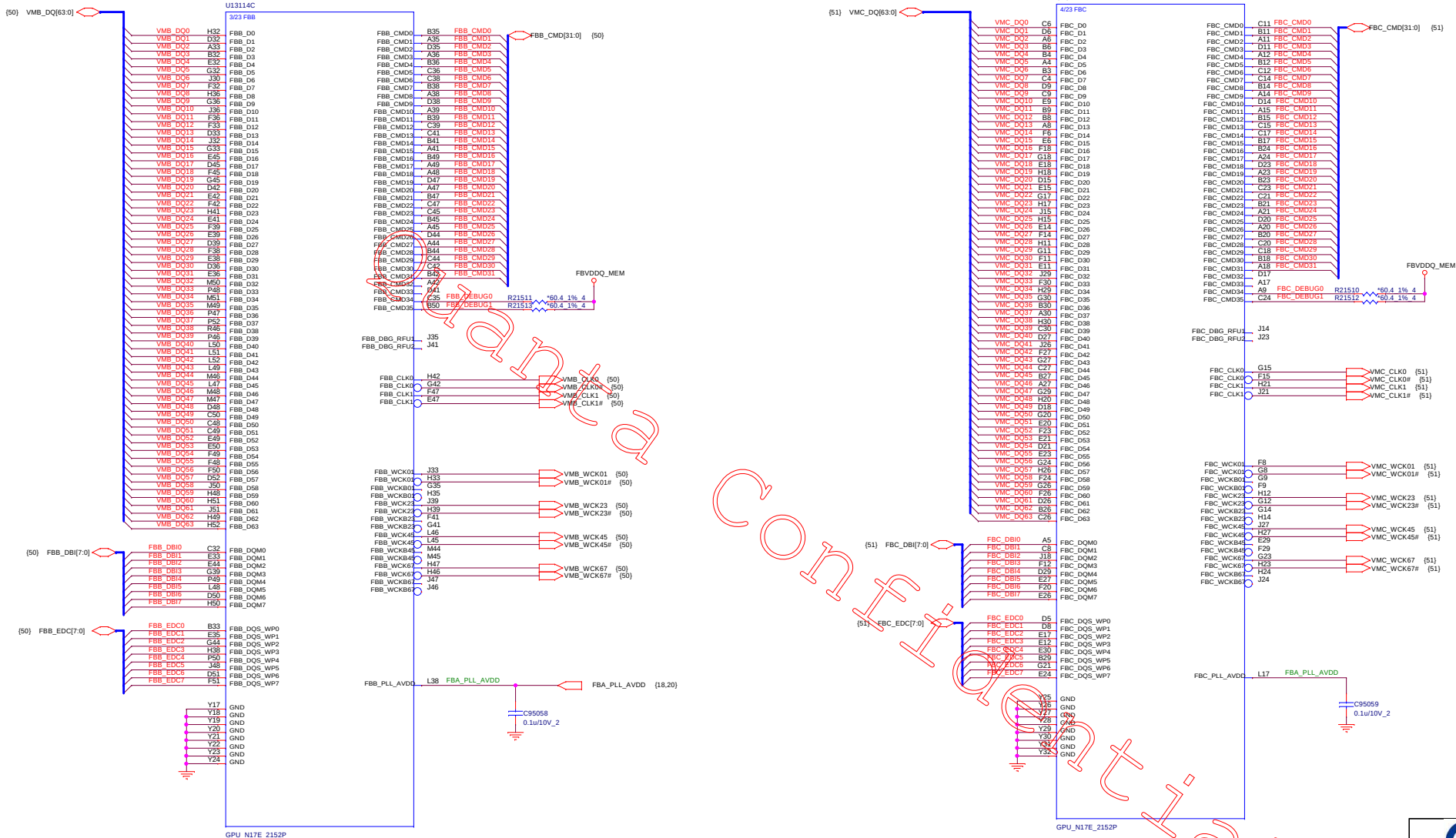

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Size	Document Number	Rev
	N17E-GX-2/9 (Memory)_1	3A

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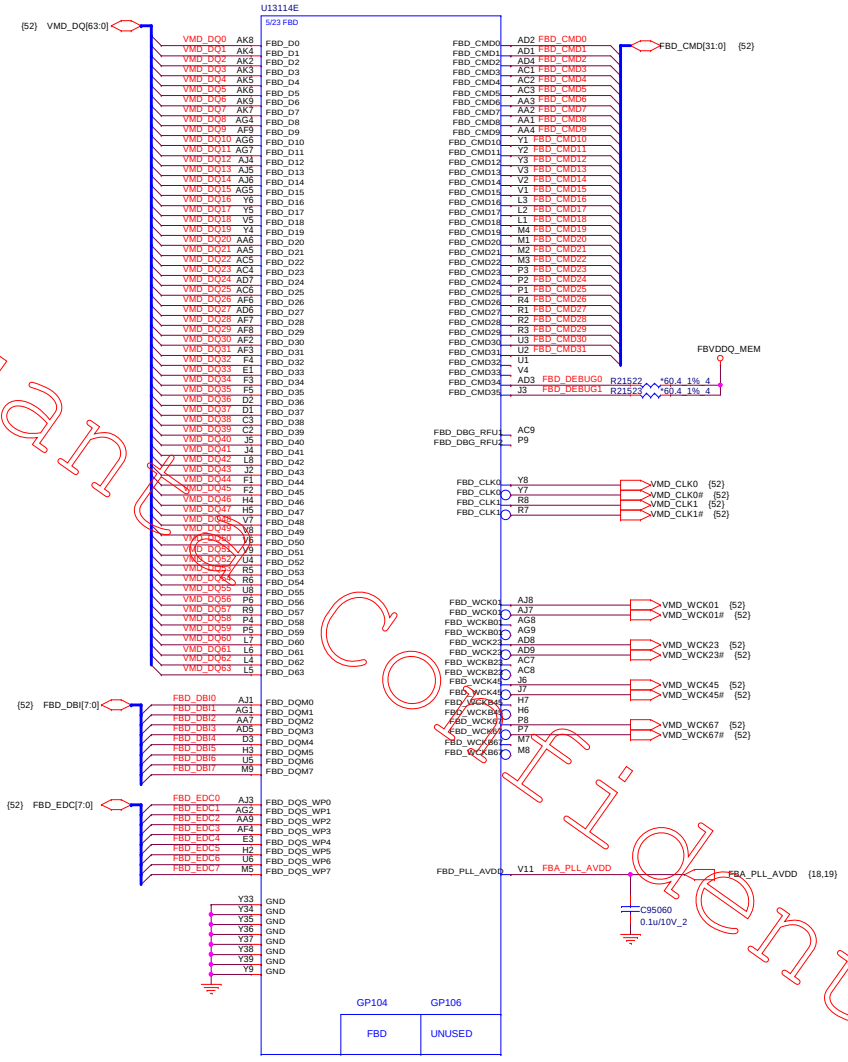

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Size	Document Number	Rev
	N17E-GX-3/9 (Memory)_2	3A

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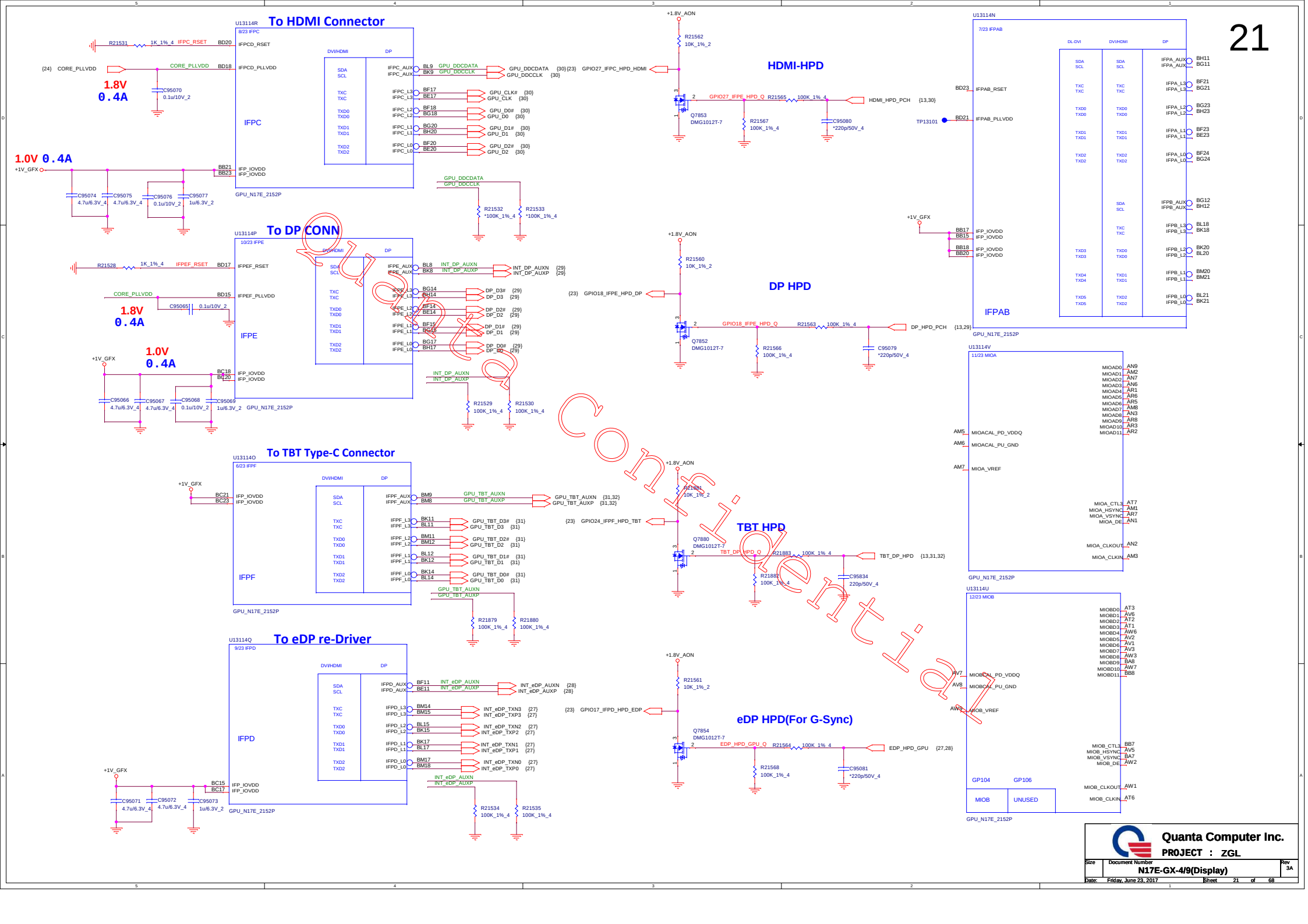
To HDMI Connector
To DP CONN
To TBT Type-C Connector
To eDP re-Driver
HDMI-HPD
DP HPD
TBT HPD
eDP HPD(For G-Sync)
U13114R
U13114P
U13114O
U13114Q
U13114N
U13114V
U13114U
IFPC
IFPE
IFPF
IFPD
IFPAB
GPU_N17E_2152P
1.8V 0.4A
1.0V 0.4A
+1.8V_AON
+1V_GFX
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Table 5.3 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

VRAM Table

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N	
0x0	GDDR5X 256Mx32 8 GHz	Micron A die	MT58k256M32-100:A			

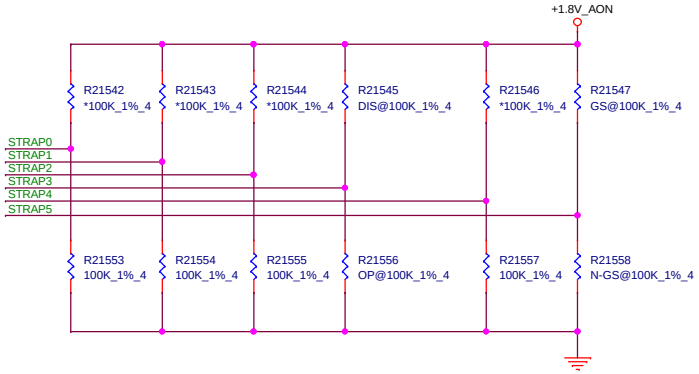
Table 4. N17E-G3 GDDR5X Recommended Memories

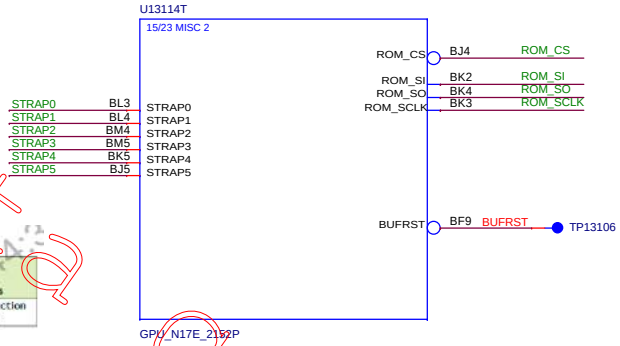
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1..35V	Micron	MT58K256M32 -100:A	A-die	0x0	10 Gbps	N/A	Full	Production ready

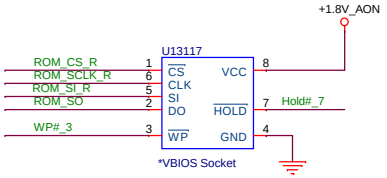
Table 1. N17E-G1/-G2 GDDR5 Recommended Memories

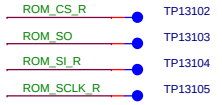
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.55V	Samsung	K4G80325FB-HC25	B-die	0x0	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V	Micron	MT51J256M32HF-80:A	A-die	0x1	8 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V	Hynix	H5GQ8H24MJR-R4C	M-die	0x2	8 Gbps	N/A	Full	Post production candidate

Notes:
1. For N17E-Gx, the maximum allowable memory case temperature is 95 °C, as these are our highest end flagship GPUs.
2. N17E-Gx runs WCLK up to 3000 MHz with FBVDD=1.35V. 1.45 is required to run WCLK > 3000 MHz.

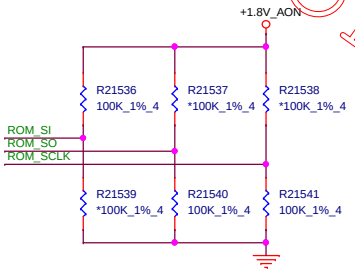


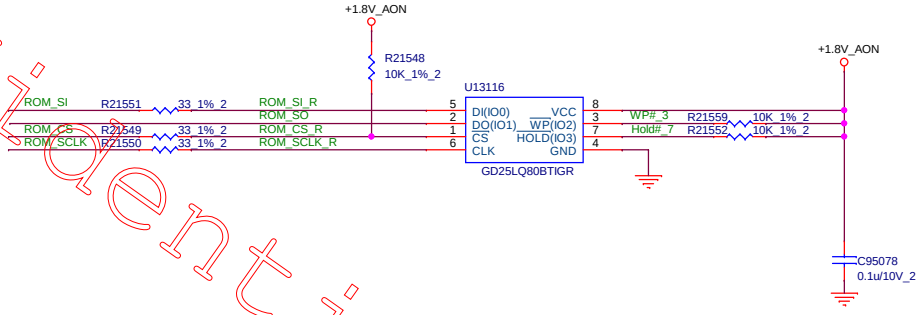






For ICT test





	STRAP5
G-SYNC	100K PU
None G-SYNC	100K PD

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Morris Chiu NVIDIA Confidential 2016-04-06 22:50:44
Mt2 - HP Notebook 2016-04-06 22:50:44

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	N17E-GX-5/9(Strap)	3A

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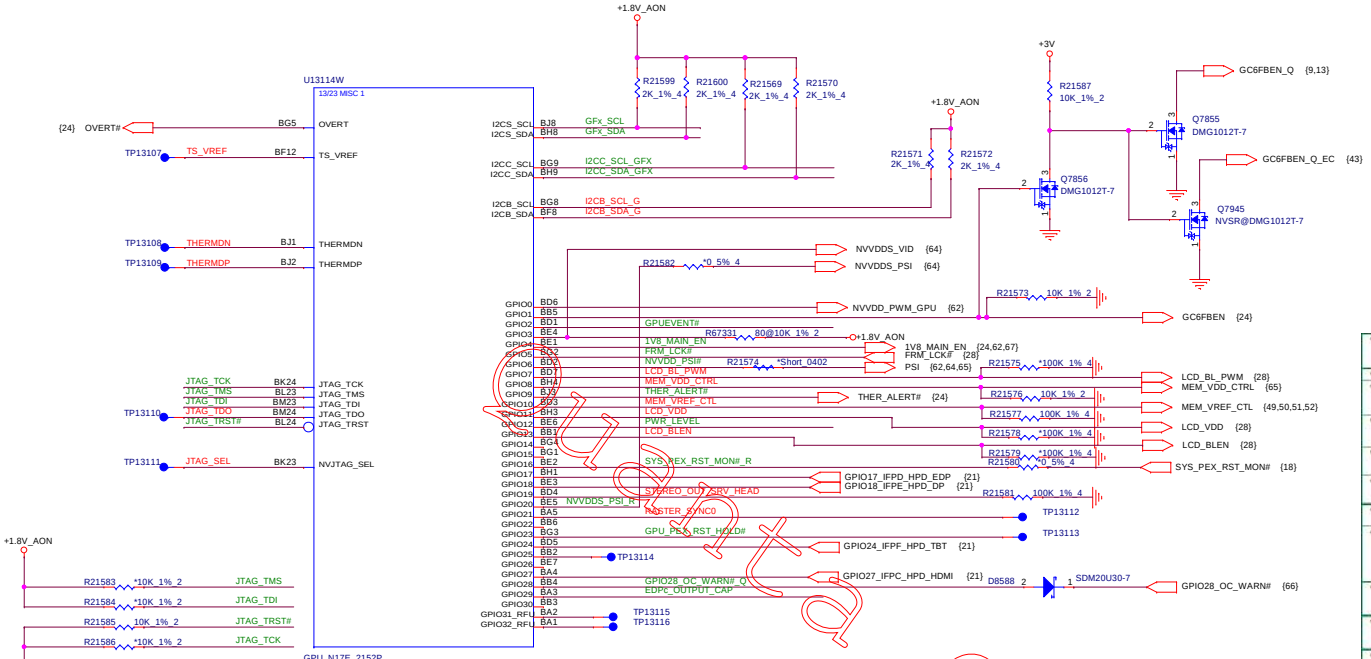

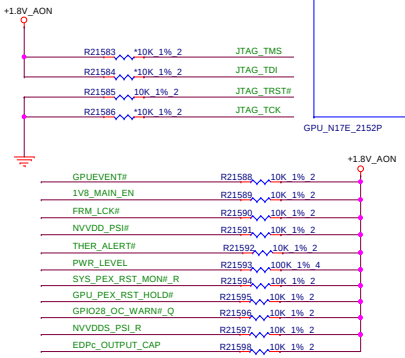

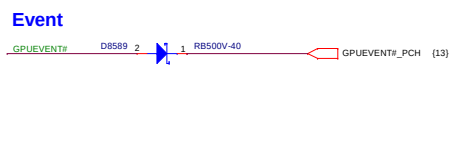

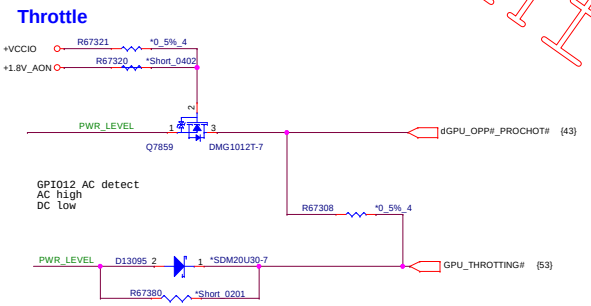

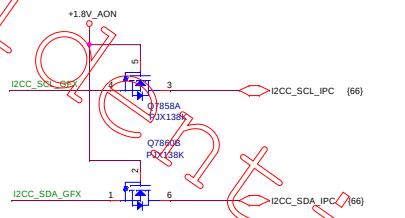

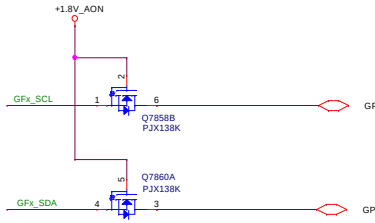

Table 14.3 GPIO Descriptions for GB4-256 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V5 PWM output
GPIO1	GC6M: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6M: GPU_EVENT#/ WAKE#	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6M: 1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.3.3)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable Control signal to turn on a logo LED	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro Power Brake#	O	Turn on heat sink logo LED when present Panel Power enable	10K pull-up to a gated 3V3 100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply max draw input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable/Fan Tachometer, see Section 14.3.9.	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6M: SYS_PEX_RST_MON#	O	PWM output used to control Fan Speed see Section 14.3.9 for definition System side PCIe reset monitor	10K pull-up to a gated 3V3 10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE		Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D Vision/STEREO	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	NVVDDS_PSI OC5_MODE			
GPIO21	RASTER_SYNC0	I/O	Input when master GPU or Output when Slave GPU	100K pull-down
GPIO22	SWAP_RDY0 or SWAPRDY_IN	I/O	SLI SWAP READY OUT	
GPIO23	GC6M: GPU_PEX_RST_HOLD#	I/O	GPU PCIe self-reset control input when master GPU or Output when Slave GPU (SLI with more than 2 boards only)	Open Drain 10 kΩ pull-up to a gated 3V3 100K pull-down
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED	I/O		
GPIO26	UNUSED	I/O		
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5
GPIO28	OC_WARN#HT	I	Over current throttling trigger 1	10 kΩ pull-up to 1V8_AON
GPIO29	EDPc_OUTPUT_CAP	I	Input from power supply. 0 to 1V8	
GPIO30	UNUSED	I/O		

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

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Micro-Star INT'L CO., LTD. MS-17B1 Schematics Document
Quanta NP Notebook Schematics Document
Wistron Corporation Schematics Document
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Size	Document Number	Rev
	N17E-GX-6/9(GPIO)	3A

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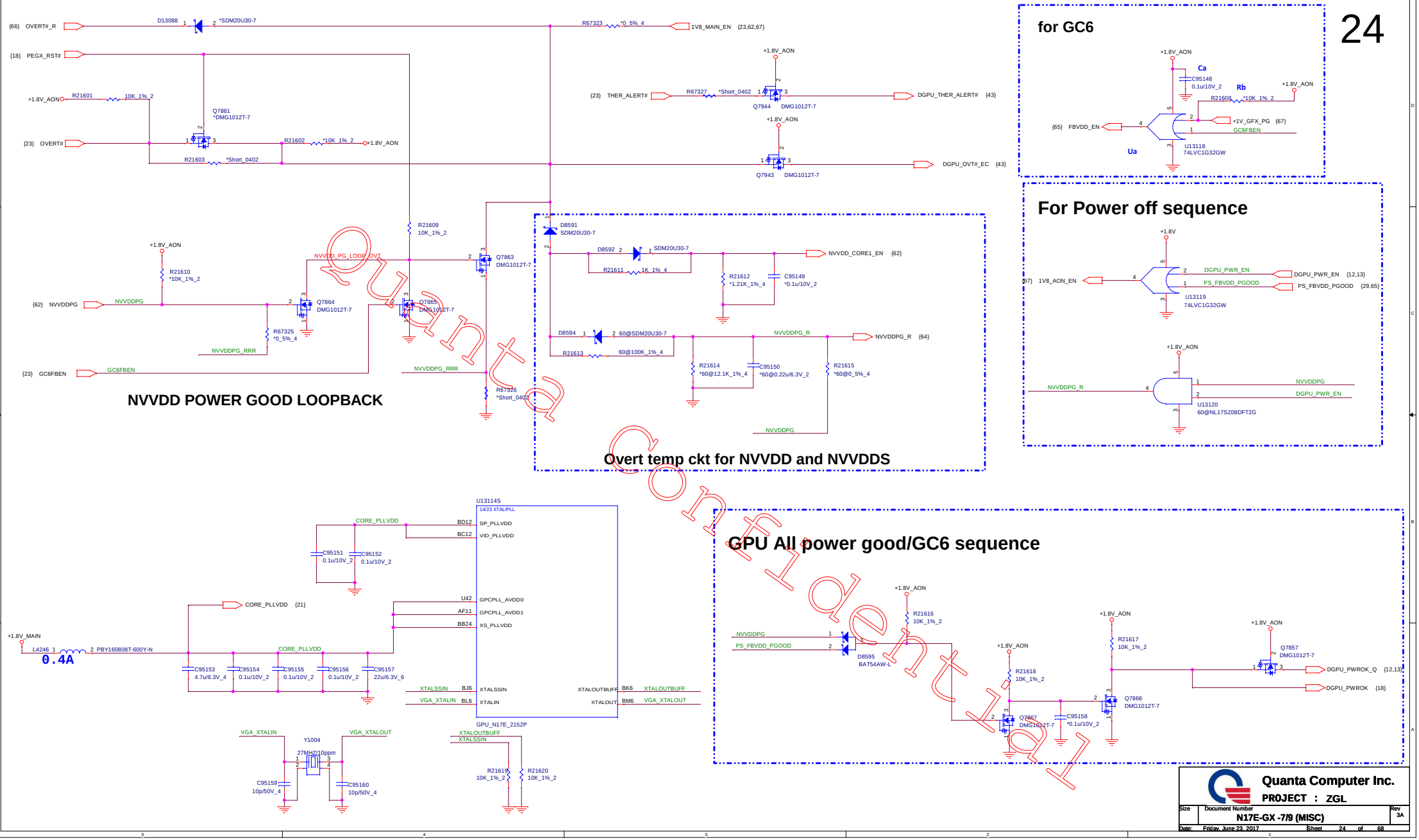

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	N17E-GX -7/9 (MISC)	3A
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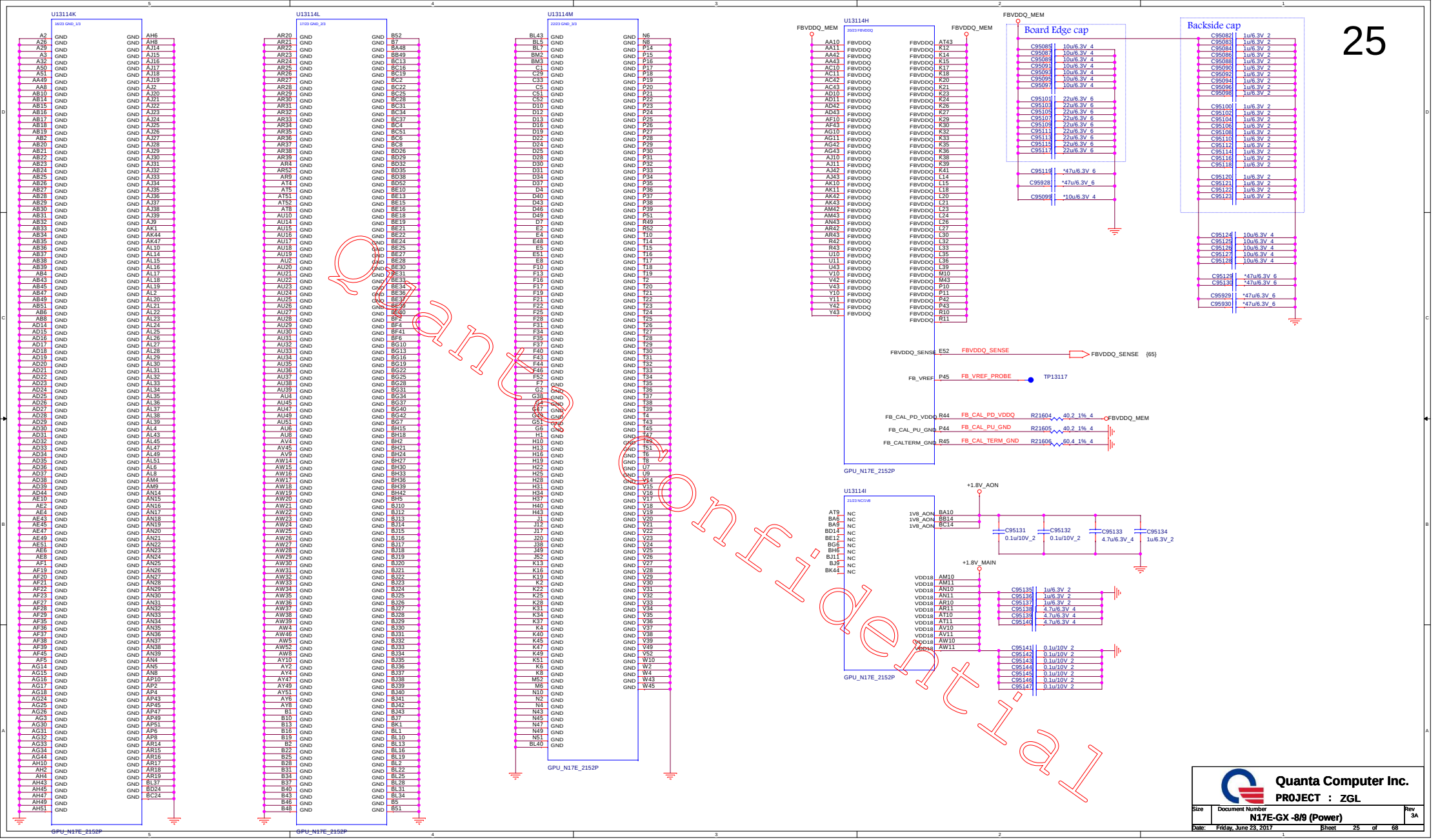

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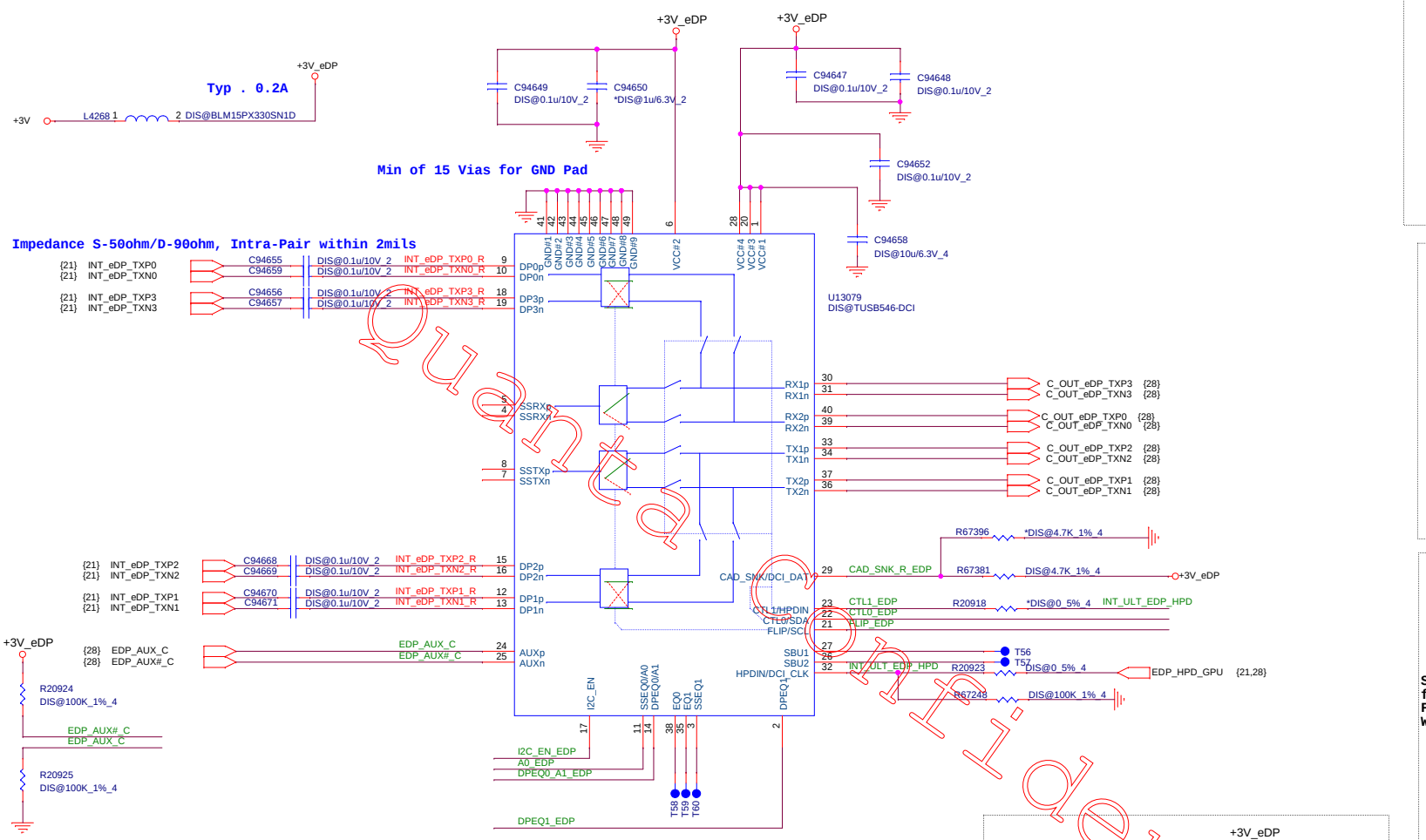

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

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EDP Optimus/Discrete

LCD CONNECTOR

LCD Power

Backlight

Hall Sensor (HSR)

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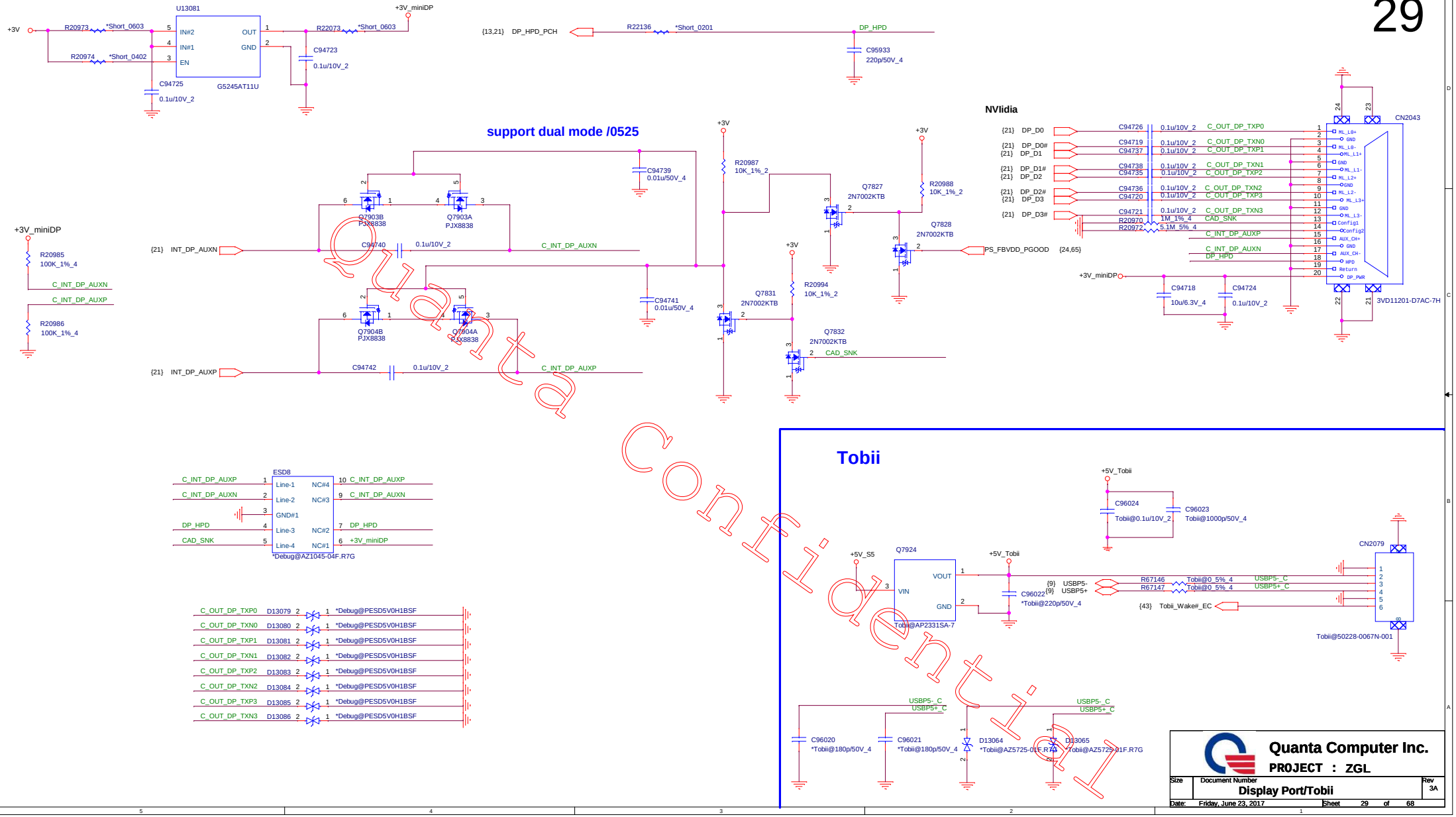

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	Display Port/Tobii	3A

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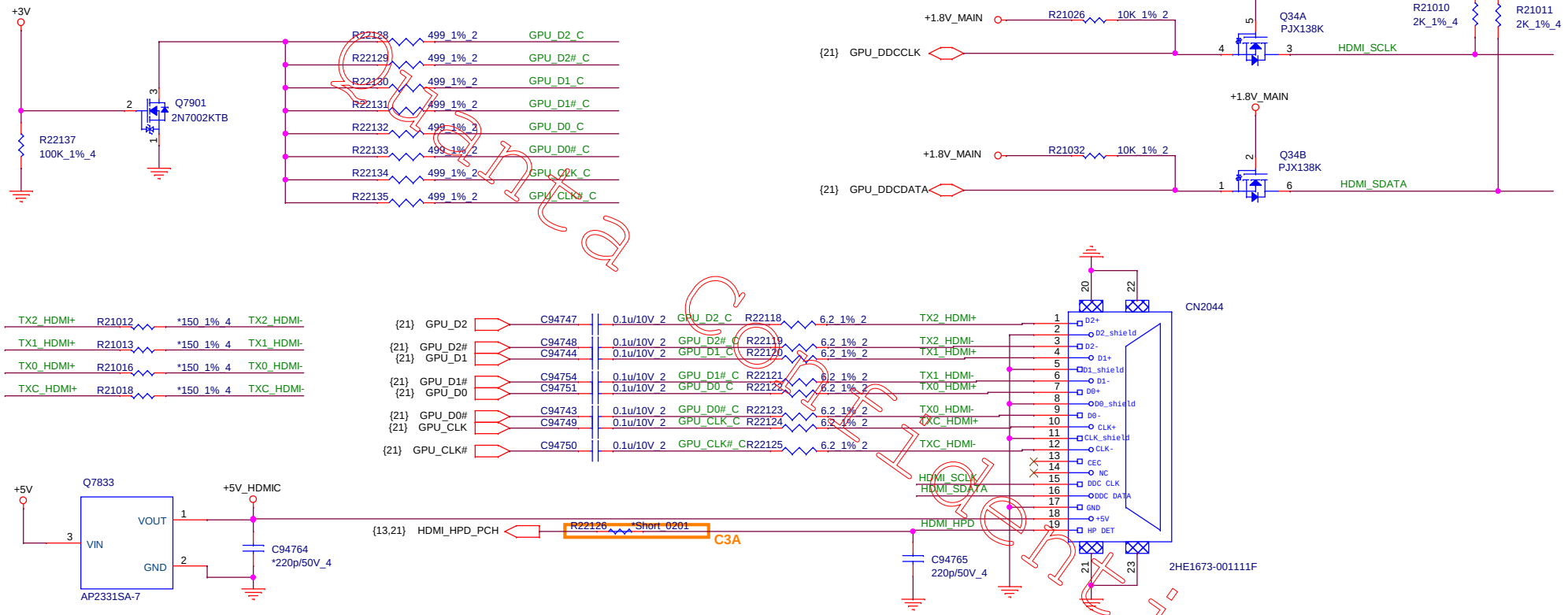
HDMI LEVEL SHIFT



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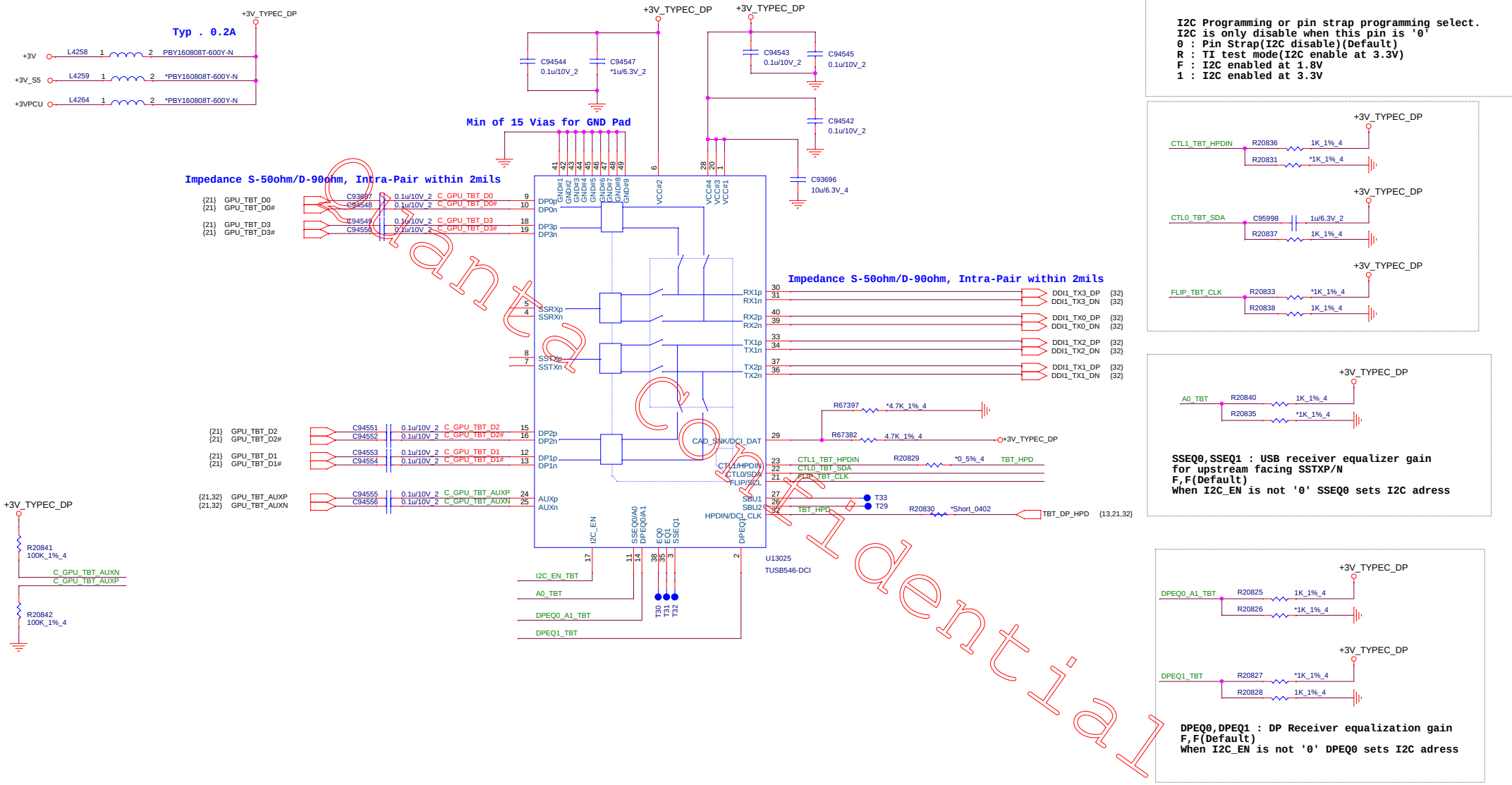

I2C Programming or pin strap programming select.
I2C is only disable when this pin is '0'
0 : Pin Strap(I2C disable)(Default)
R : TI test mode(I2C enable at 3.3V)
F : I2C enabled at 1.8V
1 : I2C enabled at 3.3V

SSEQ0,SSEQ1 : USB receiver equalizer gain for upstream facing SSTXP/N
F,F(Default)
When I2C_EN is not '0' SSEQ0 sets I2C adress

DPEQ0,DPEQ1 : DP Receiver equalization gain
F,F(Default)
When I2C_EN is not '0' DPEQ0 sets I2C adress

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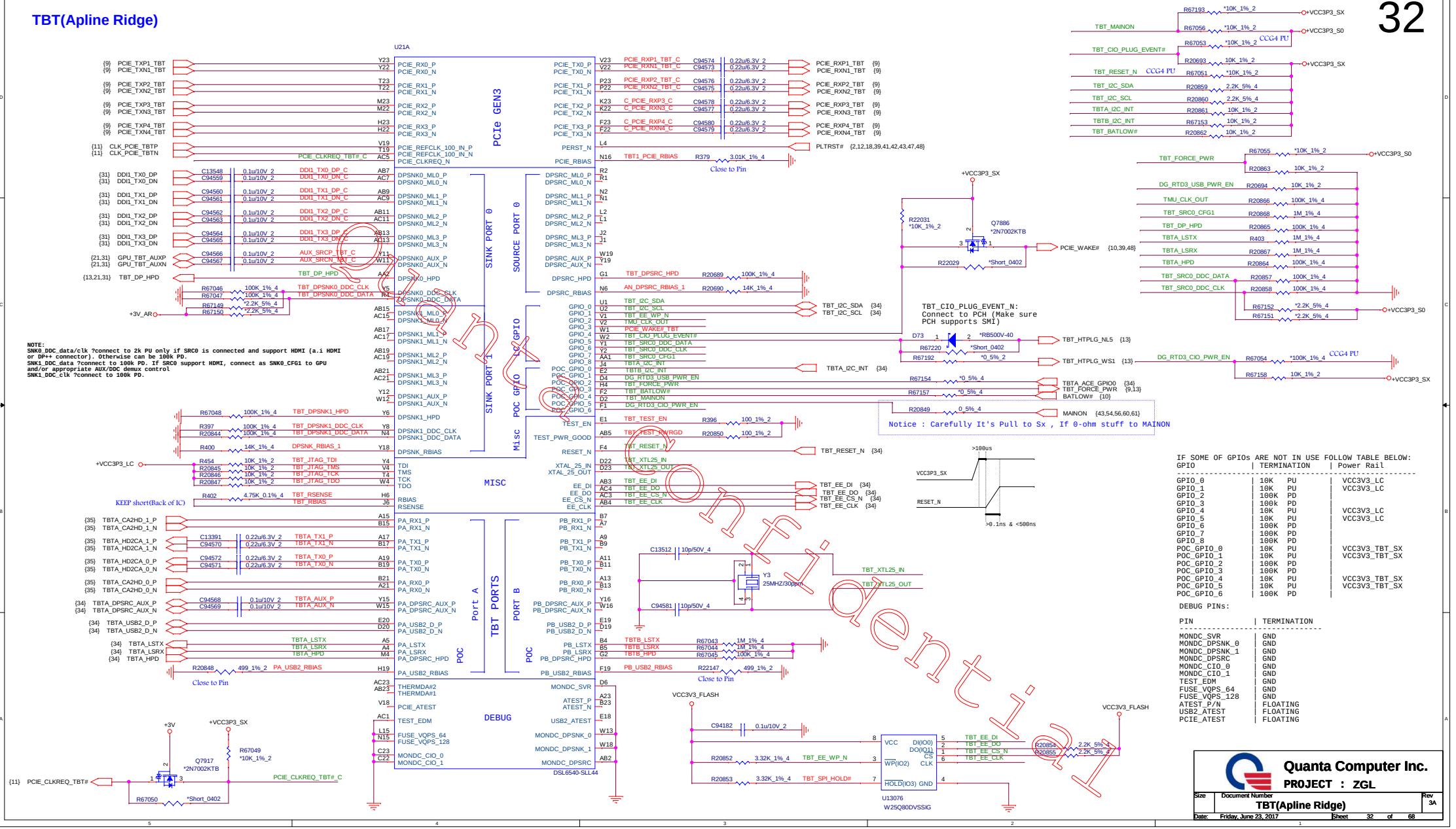
TBT(Apline Ridge)



NOTE:
SNK0_DDC_data/clk ?connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PD.
SNK1_DDC_data ?connect to 100k PD. If SRC0 support HDMI, connect as SNK0_CFG1 to GPU and/or appropriate AUX/DDC demux control
SNK1_DDC_clk ?connect to 100k PD.

IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	
GPIO_3	100k PD	
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	
GPIO_7	100K PD	
GPIO_8	100K PD	
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	
POC_GPIO_3	100K PD	
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	

DEBUG PINs:

PIN	TERMINATION
MONDC_SVR	GND
MONDC_DPSNK_0	GND
MONDC_DPSNK_1	GND
MONDC_DPSRC	GND
MONDC_CIO_0	GND
MONDC_CIO_1	GND
TEST_EDM	GND
FUSE_VQPS_64	GND
FUSE_VQPS_128	GND
ATEST_P/N	FLOATING
USB2_ATEST	FLOATING
PCIE_ATEST	FLOATING

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TBT(Apline Ridge Power)

NOTE1

40KHz LC Filter to reduce VCC3v3_S0_TBT ripple

L (LQM18PN1R0MFHD):
RDC < 0.2Ohm
IDC > 0.2A

C (GRM188R60J476ME15):
Need to notice the capacitance at 3.3 Vdc

NOTE3

Share Same GND plane with SVR_VSS of AR

NOTE3

Inductor value should be 0.6uH or 0.68uH
DCR should be as low as possible; 20mΩ – 25mΩ or lower
Saturation current should be above 5A

NOTE2

Option 1 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R3>. Keep <R2> empty.
2. Make sure VCC3v3_SX_SYS can support AR maximum power consumption.
3. Simple Bios implementation

Option 2 for wake support over TBT:
1. Connect 0Ohm to <R1> and <R2>. Keep <R3> empty.
2. Bios need to implement Sx entry pre-notice flow by PCIe2TBT.

No wake support at all from AR
1. Connect 0Ohm to <R2> and <R3>. Keep <R1> empty.

<S5>
Acer S5 is off on AC/DC

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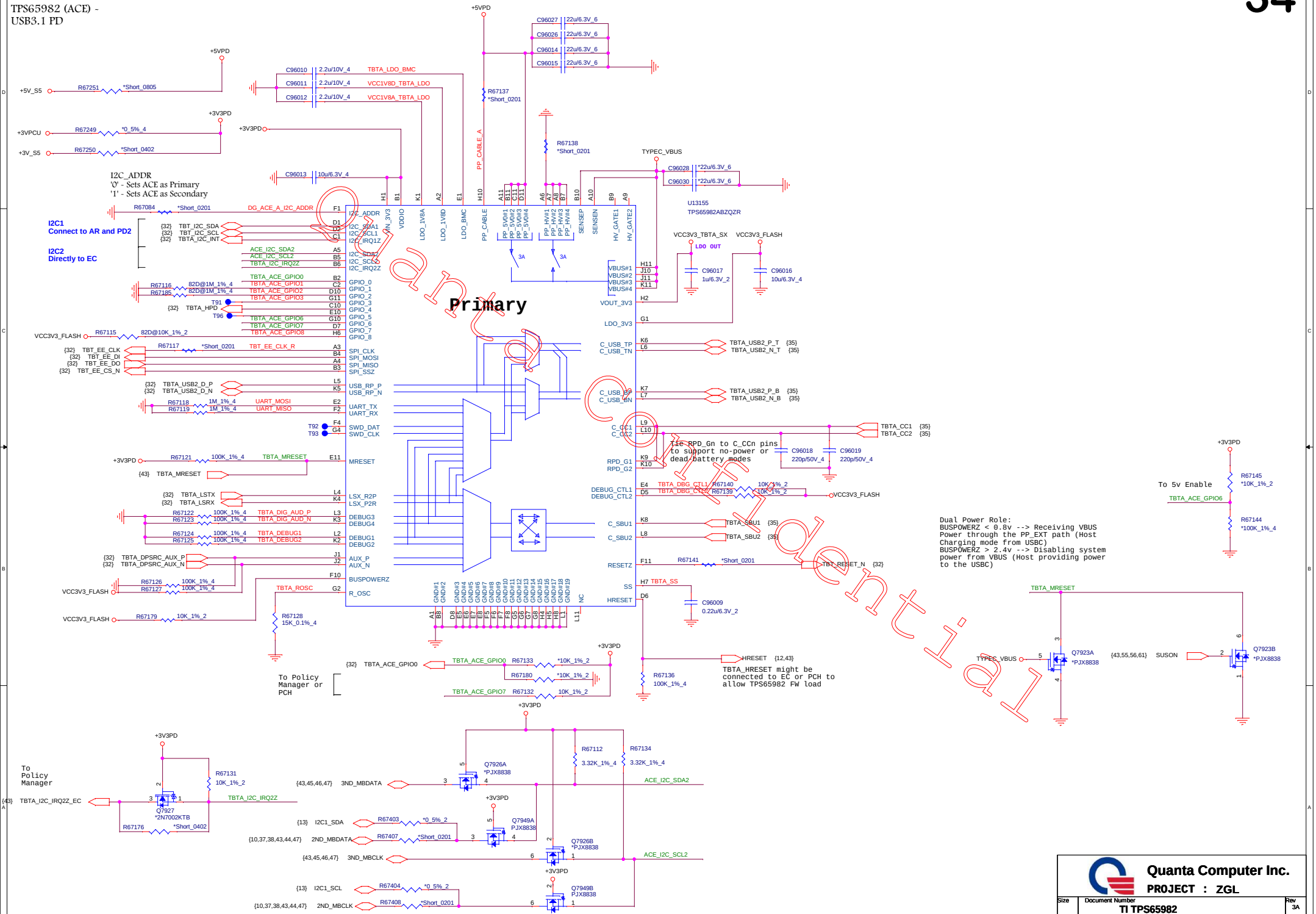
Port A Controller - ACE

TPS65982 (ACE) -
USB3.1 PD



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	TI TPS65982		3A
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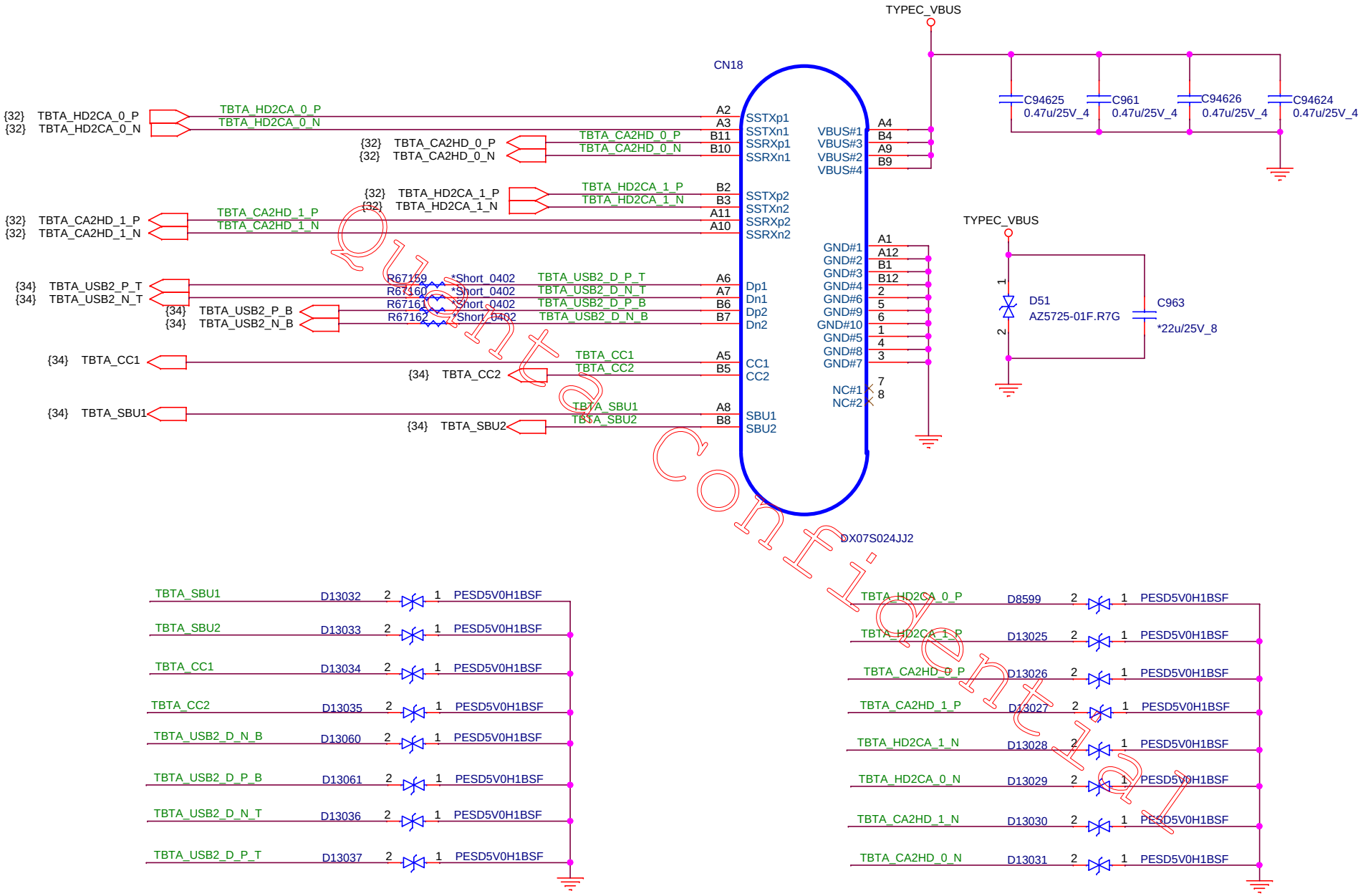

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	Type C(USB3.1/DP) *1	3A
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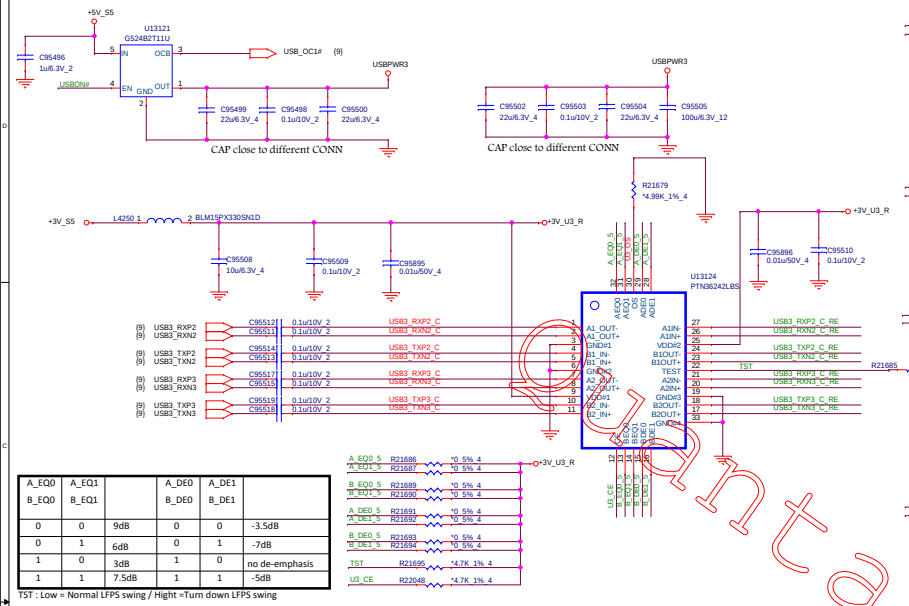
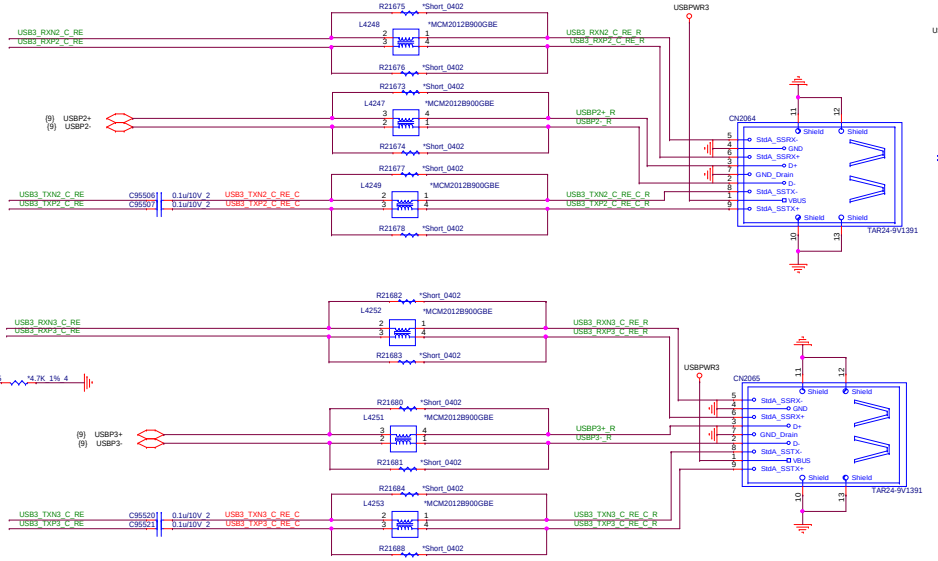
USB 3.0(UB3) -Left

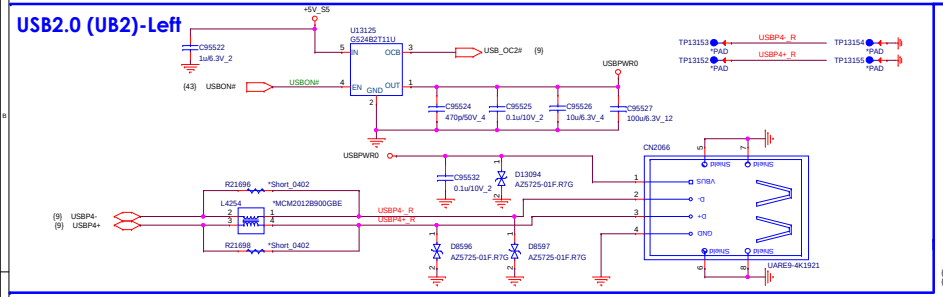


A_EQ0 B_EQ0	A_EQ1 B_EQ1		A_DE0 B_DE0	A_DE1 B_DE1	
0	0	9dB	0	0	-3.5dB
0	1	6dB	0	1	-7dB
1	0	3dB	1	0	no de-emphasis
1	1	7.5dB	1	1	-5dB

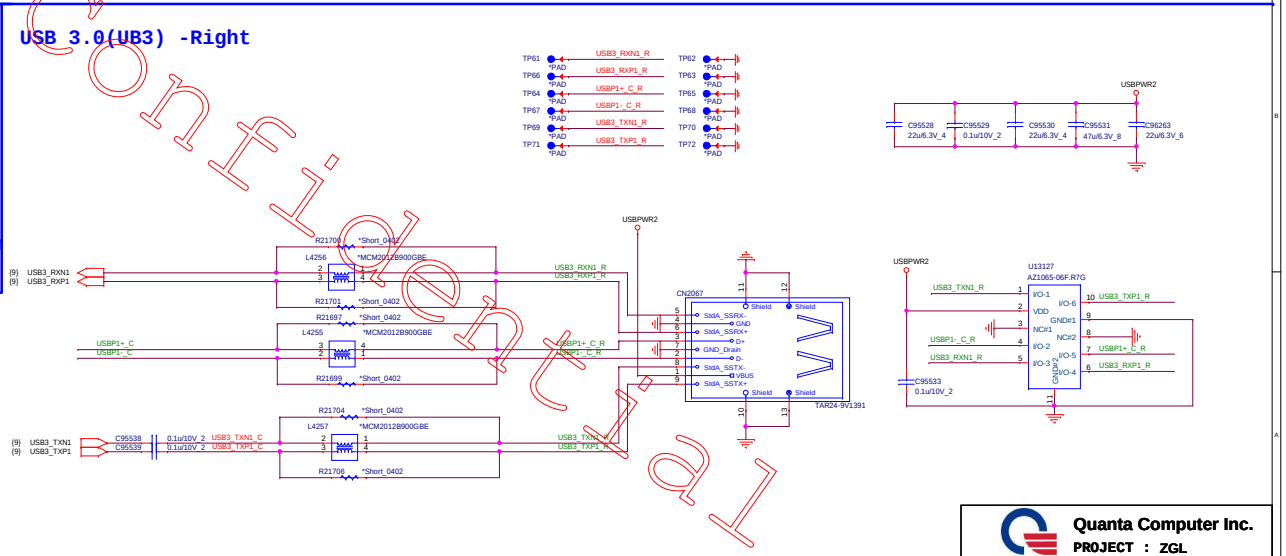
TST : Low = Normal LFPS swing / Hight =Turn down LFPS swing



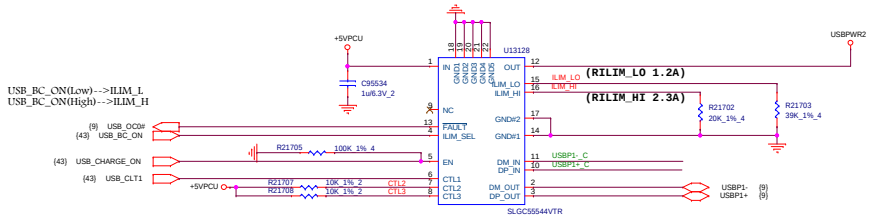
USB2.0 (UB2)-Left



USB 3.0(UB3) -Right



BC1.2 -U3 OF Right side



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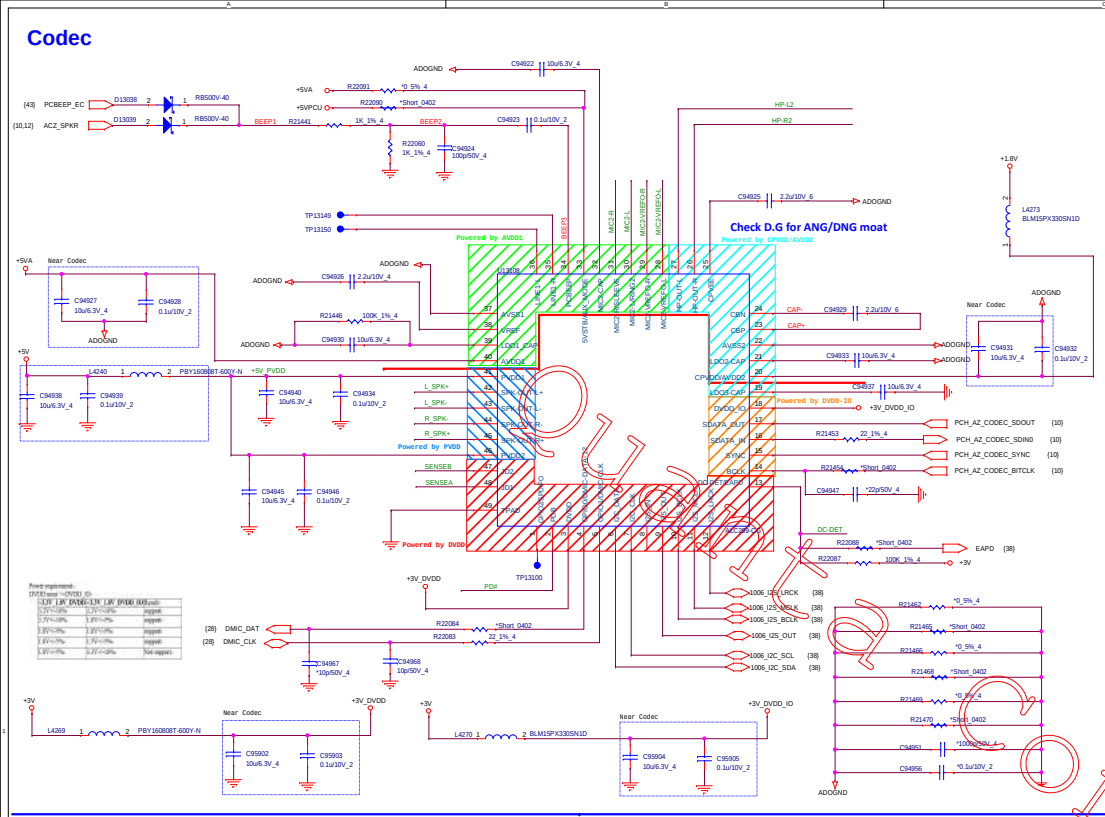
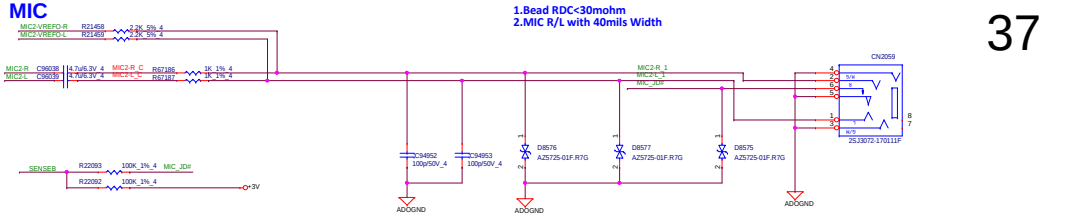
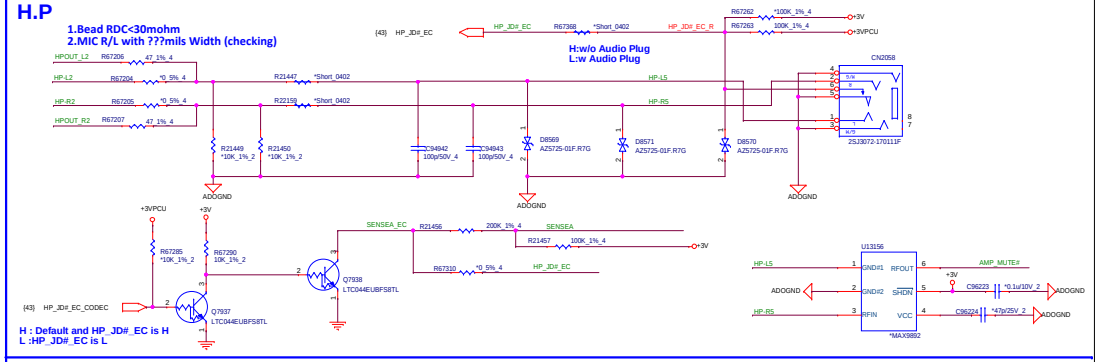
Codec



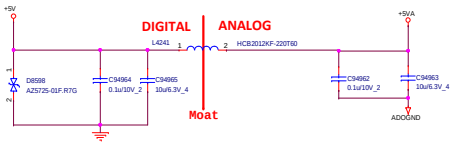
MIC



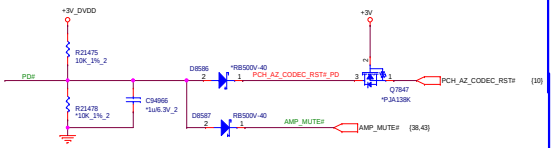
H.P



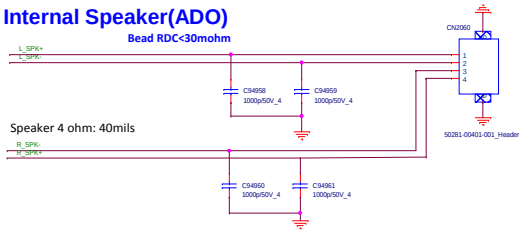
Codec PWR 5V(ADO)



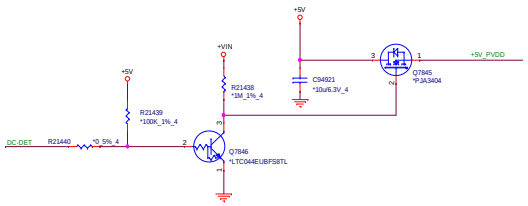
Mute(ADO)



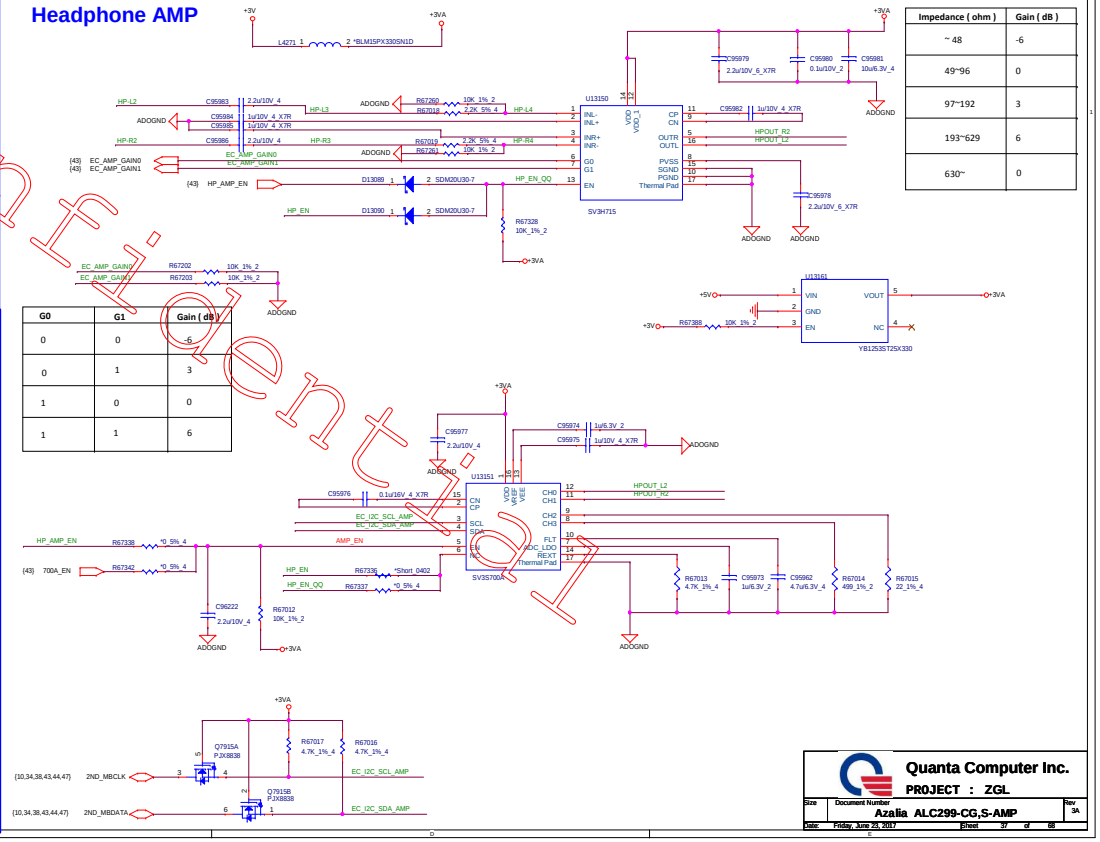
Internal Speaker(ADO)



DC-DET circuit(ADO)



Headphone AMP



Impedance (ohm)	Gain (dB)
~ 48	-6
49~96	0
97~192	3
193~629	6
630~	0

G0	G1	Gain (dB)
0	0	-6
0	1	3
1	0	0
1	1	6

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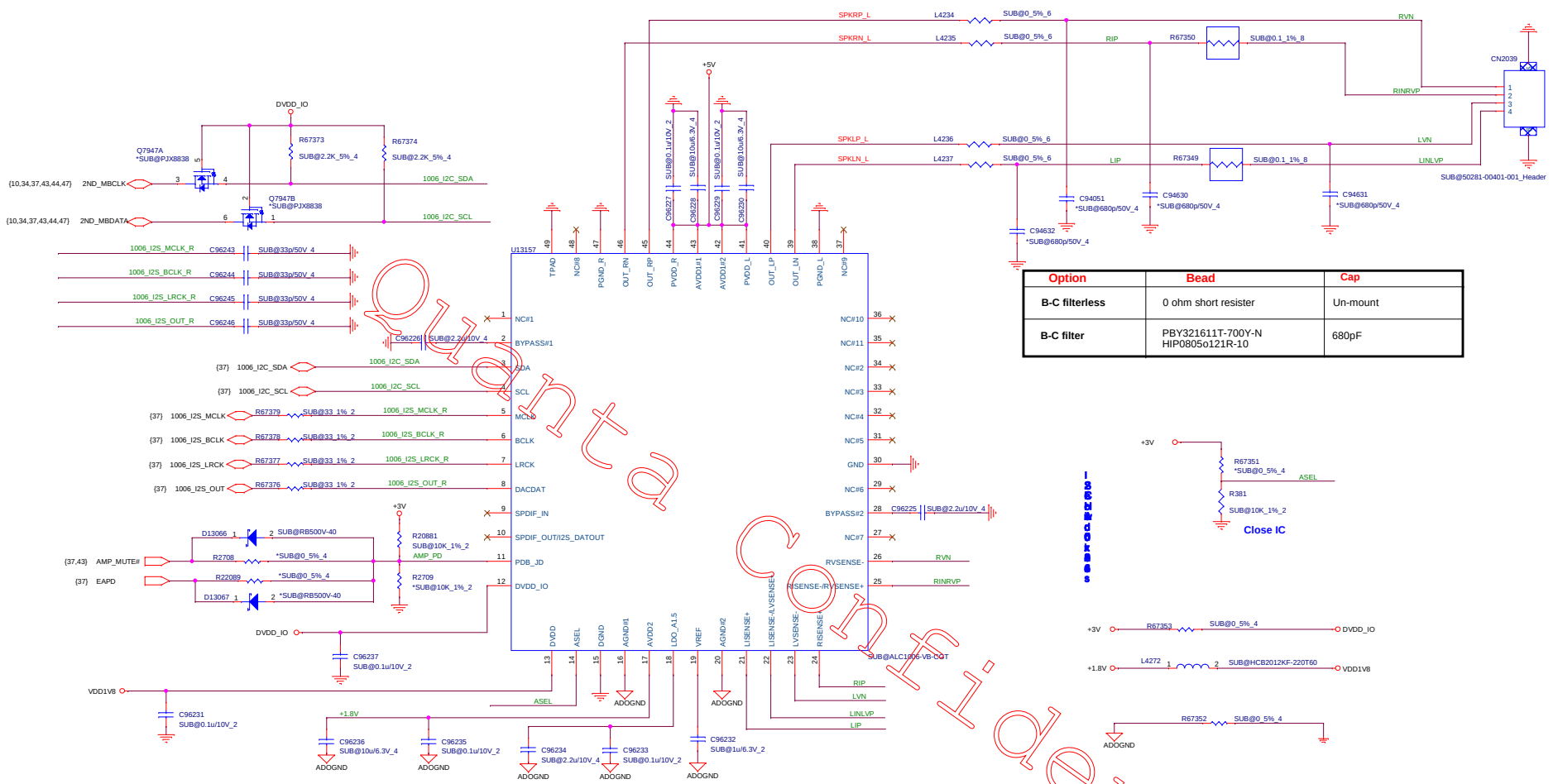
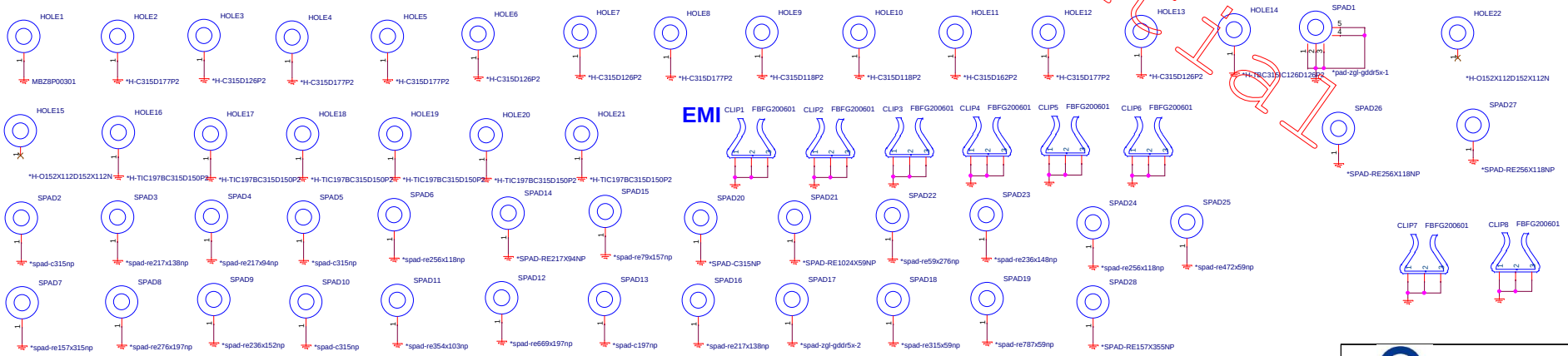
SubWoofer



Option	Bead	Cap
B-C filterless	0 ohm short resister	Un-mount
B-C filter	PBY321611T-700Y-N HIP0805o121R-10	680pF

Hole



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	Subwoofer(ALC105)/HOL/EMI		3A
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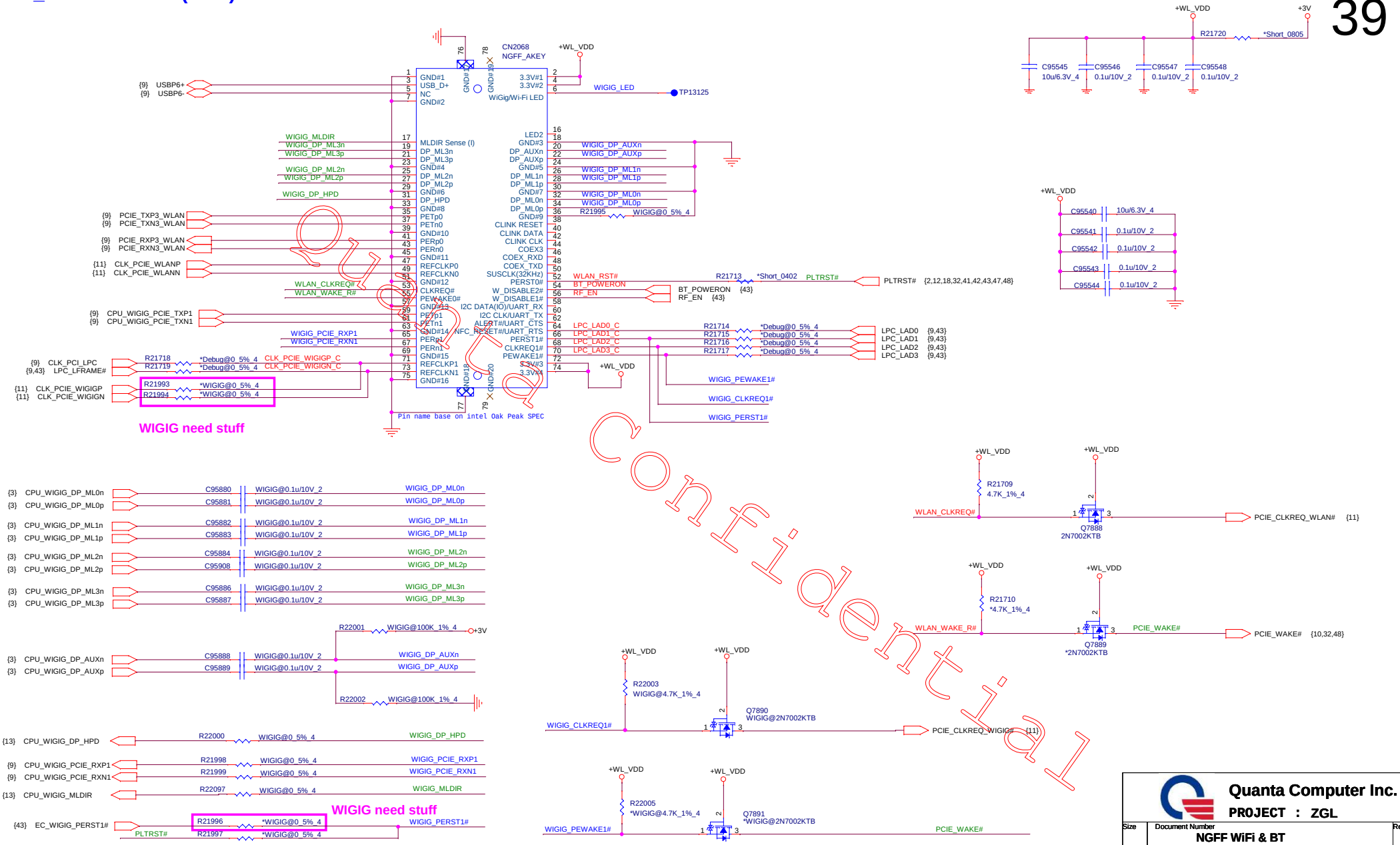
NGFF_M.2 WiFi & BT (NGF)



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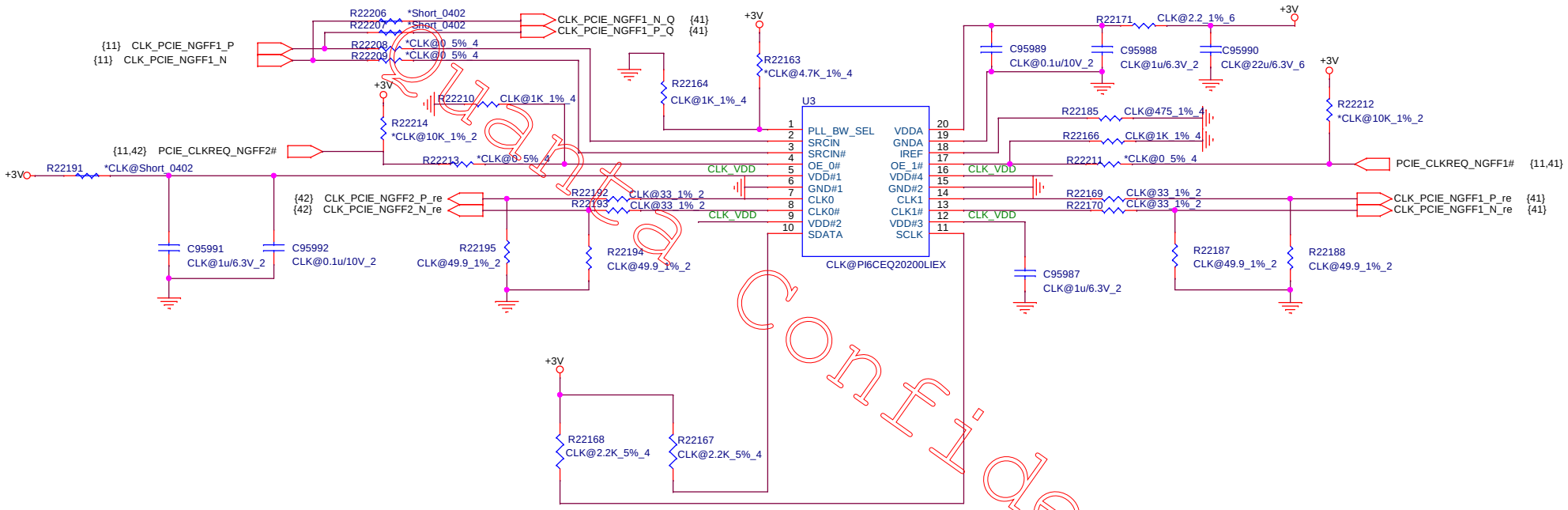
NGFF_M.2 SSD #1 #2 (NGF)



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PROJECT : ZGL

Size	Document Number	Rev
	SSD Clock re-Driver	3A
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NGFF_M.2 SSD #1 (NGF)

(SATA/ PCIE)

CN2069
NASM0-B6701-TS18

U13146
PS8559BQFN40GTR-A0

U13147
PS8559BQFN40GTR-A0

CN11
HDD@MAIN_SATA_CONN

Q7874
2N7002KTB

80 mils

PWD
L: Normal operation (default)
H: Chip power down

DE <1:0>
00 : -3.5 dB(default)
01 : -2 dB
10 : -6 dB
11 : -7.5 dB

EQ <2:0>
000 : 14 dB
001 : 10 dB
010 : 8 dB
011 : 4 dB
100 : 16 dB
101 : 17 dB
110 : 19 dB
111 : 21 dB

A_SWING/B_SWING=
L: default swing
H: Increase 10%

Mode=
L: SATA Mode
H: PCIe Mode

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Quanta Computer Inc.	PROJECT : ZGL		
Size	Document Number: NGFF SSD #1		Rev 3A
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NGFF_M.2 SSD #2 (NGF)

CN2070
NASM0-B6701-TS18

(SATA/ PCIE)

SATAPCIE[7:0]: BIOS Enable PCH IPU 20K. It's can save MOS on NGFF CONN?? CRB Check???

M.2 PEDET
PCIE: NC
SATA: GND

Q7875
2N7002KTB

U13149
PS8559BQFN40GTR-A0

U13148
PS8559BQFN40GTR-A0

PWD
L: Normal operation (default)
H: Chip power down

A_SWING/B_SWING=
L: default swing
H: Increase 10%

Mode=
L: SATA Mode
H: PCIe Mode

DE <1:0>
00 : -3.5 dB(default)
01 : -2 dB
10 : -6 dB
11 : -7.5 dB

EQ <2:0>
000 : 14 dB
001 : 10 dB
010 : 8 dB
011 : 4 dB
100 : 16 dB
101 : 17 dB
110 : 19 dB
111 : 21 dB

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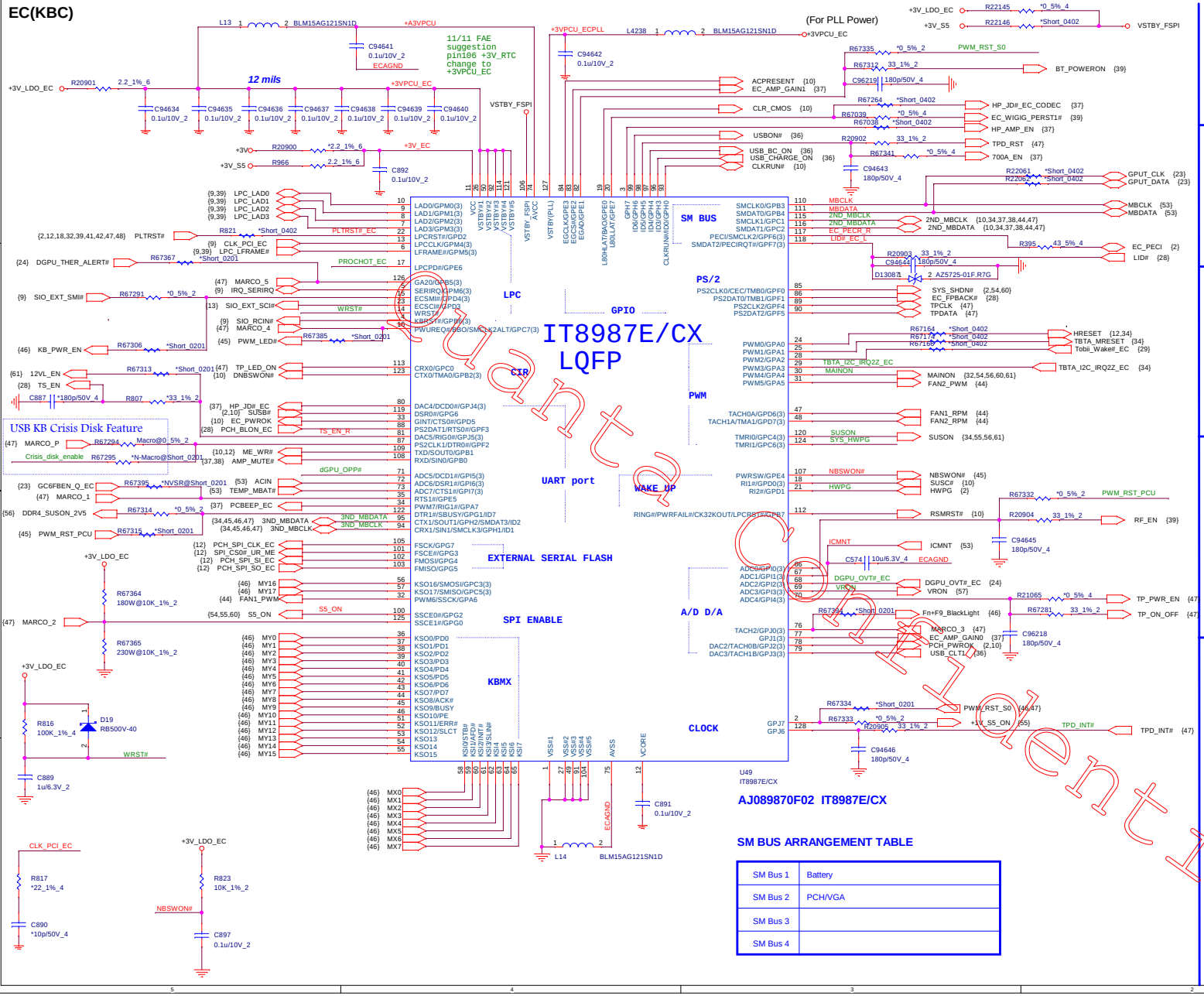
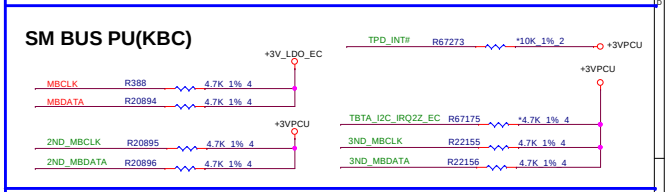
EC(KBC)



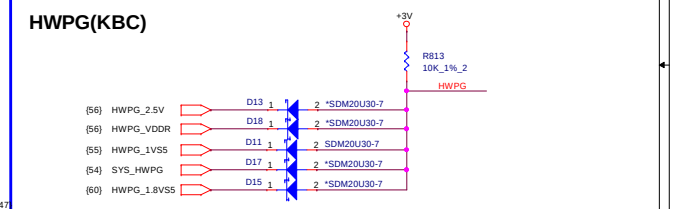
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

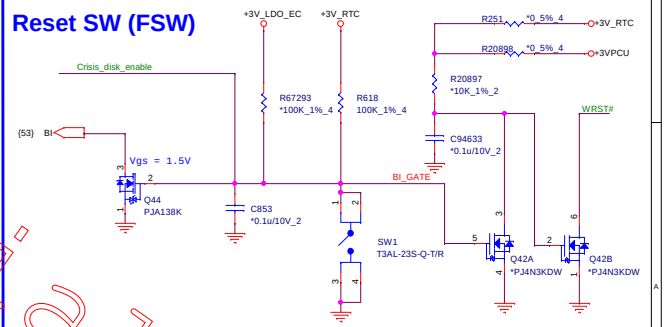
SM BUS PU(KBC)



HWPG(KBC)



Reset SW (FSW)



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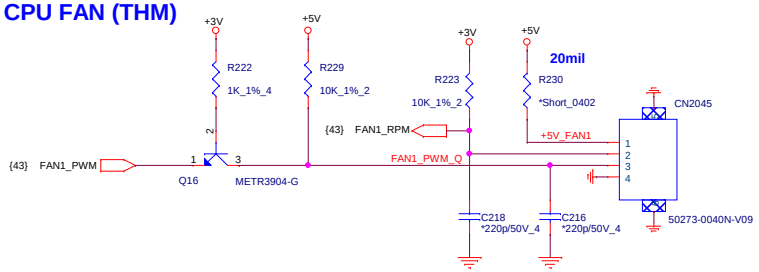
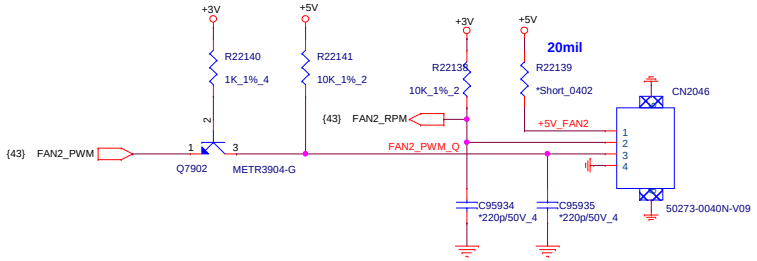
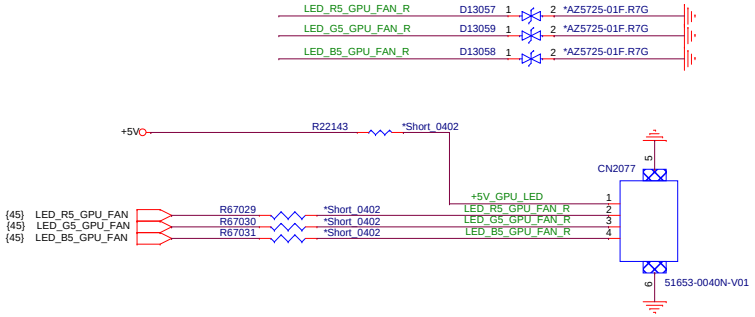
CPU FAN (THM)



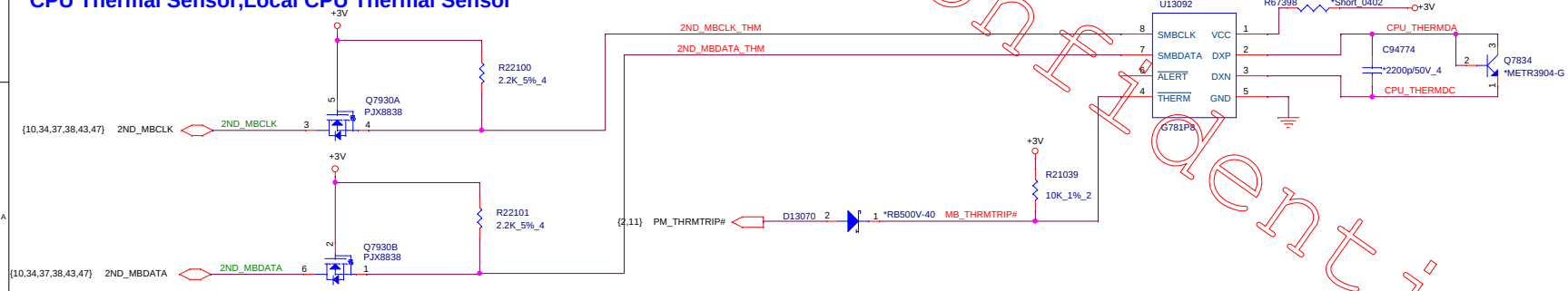
GPU FAN (THM)



GPU FAN LED



CPU Thermal Sensor,Local CPU Thermal Sensor



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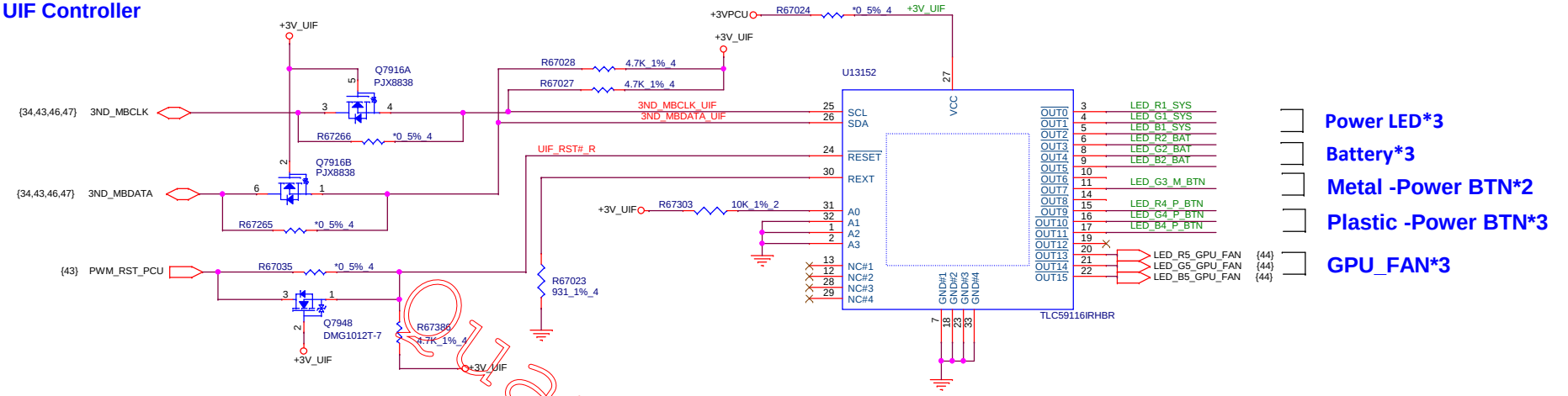
UIF Controller



Power LED*3

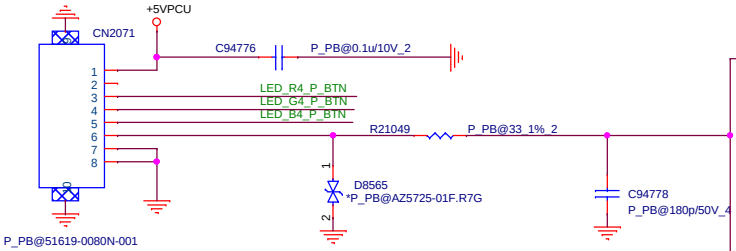
Battery*3

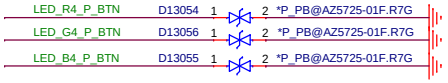
Metal -Power BTN*2

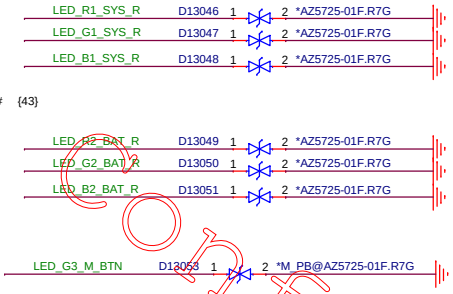
Plastic -Power BTN*3

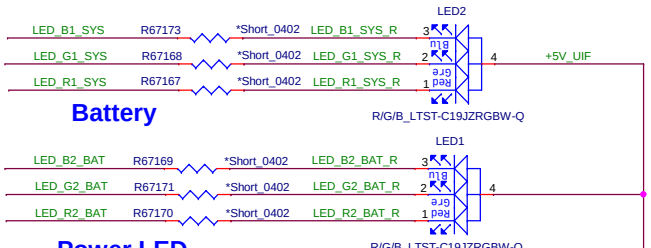
GPU_FAN*3

Plastic -Power BUTTON





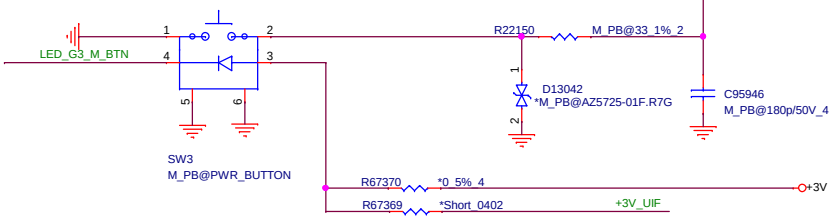


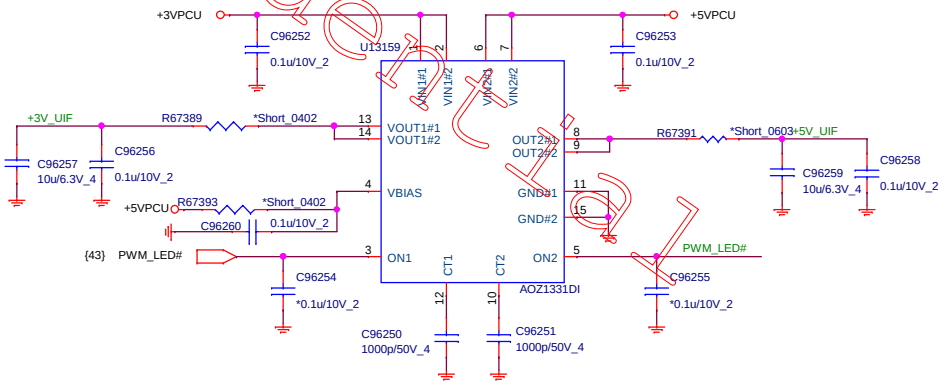


Battery

Power LED

Metal -Power BUTTON





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PROJECT : ZGL		
Size	Document Number: Power Board , UIF LED	Rev: 3A
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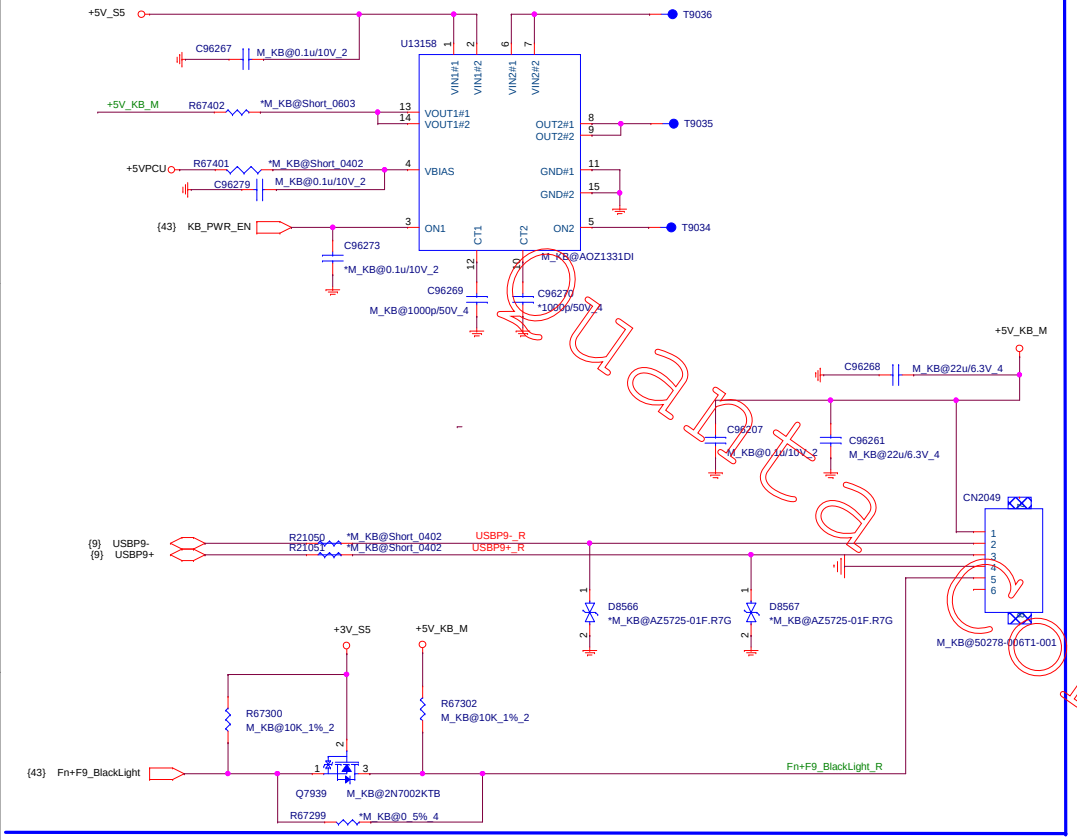
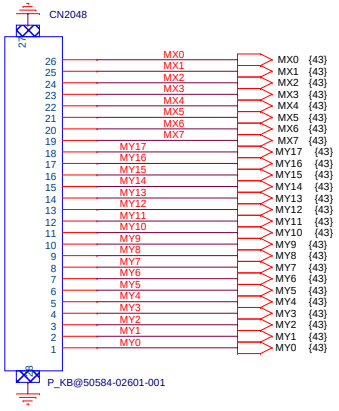
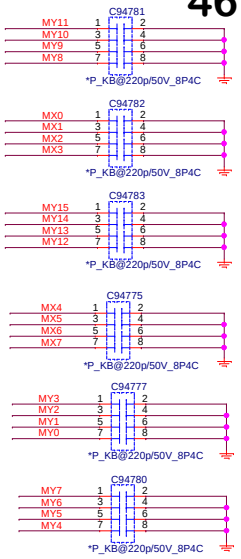
Metal KB(Z=6.8mm)

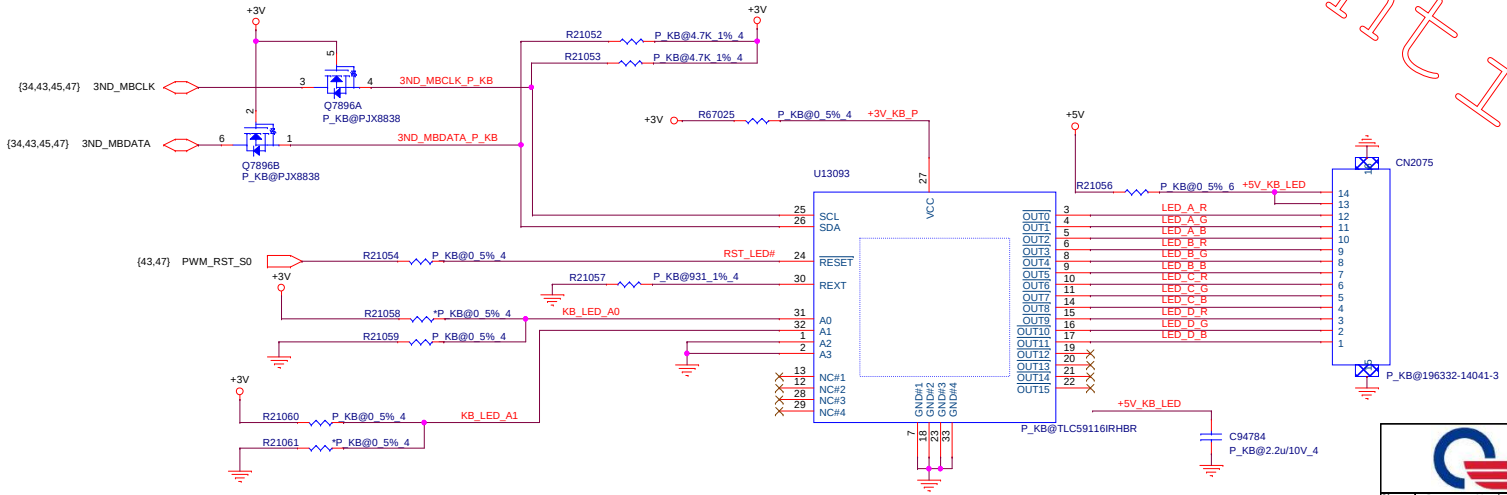


Plastic KB(Z=5.8mm)





Plastic KB(Z=5.8mm)



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PROJECT : ZGL		
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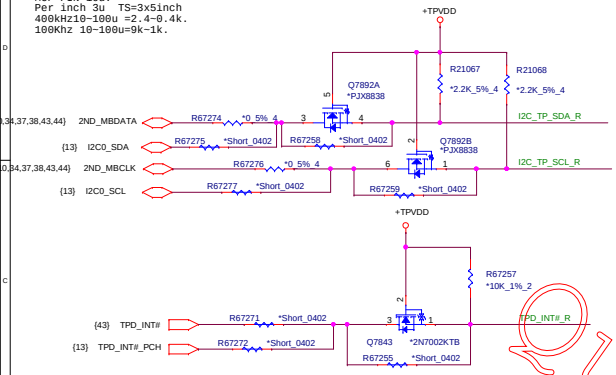
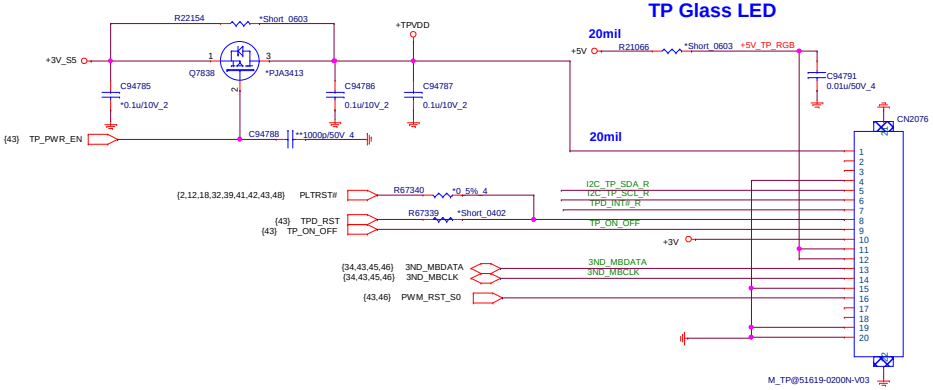
Metal-Touch PAD

```
TPD->100kHz,TS=400Khz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u  TS=3x5inch
400kHz10~100u =2.4~0.4k.
100Khz 10~100u=9k~1k.
```

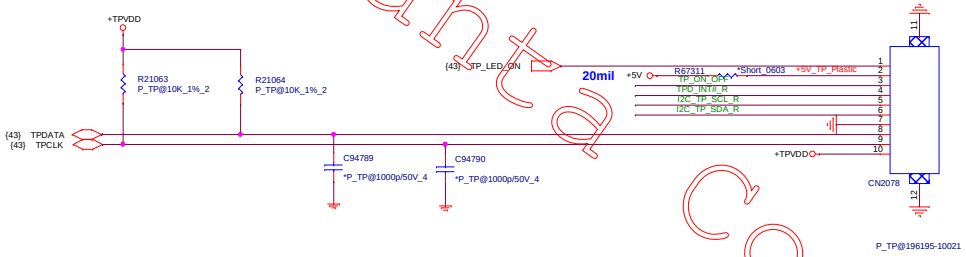


TP Glass LED

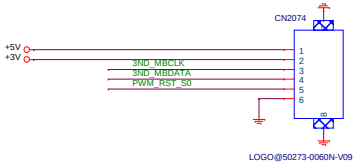


Macro Key LED

Plastic-Touch PAD



LCD Cover LED



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Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: Macro key/LCD Cover/TP	Rev 3A
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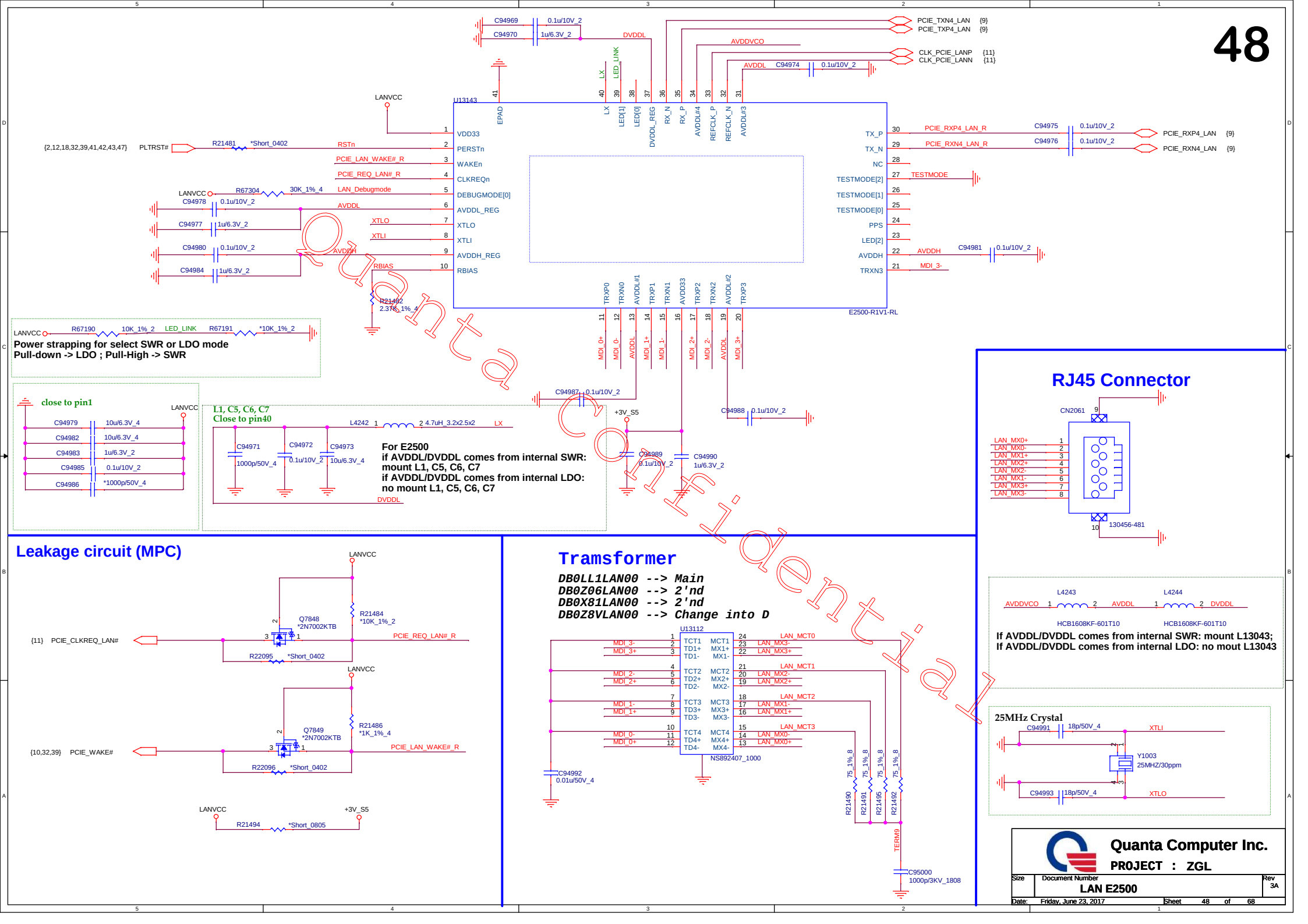

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Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	LAN E2500	3A
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CHANNEL A: 2G/4G GDDR5

Channel 0 <0-31>
MF=1 mirrored

Channel 1 <32-63>
MF=0 Non-mirrored

QD0~7

QD8~15

QD16~23

QD24~31

QD56~63

QD48~55

QD40~47

QD32~39

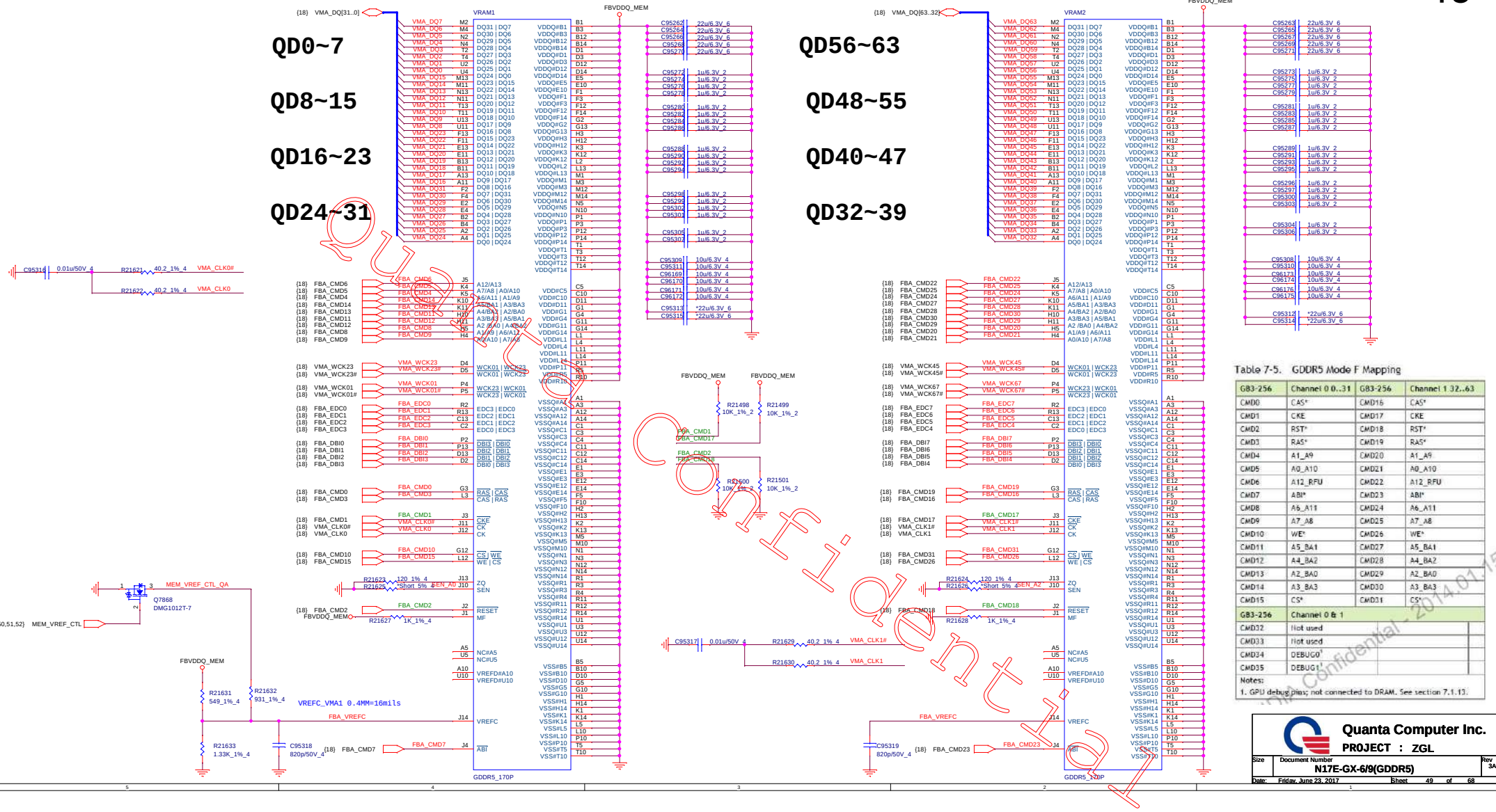

Table 7-5. GDDR5 Mode F Mapping

G83-256	Channel 0 0..31	G83-256	Channel 1 32..63
CMD0	CA5*	CMD16	CA5*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RA5*	CMD19	RA5*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
G83-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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Quanta Computer Inc.			
PROJECT : ZGL			
Size	Document Number		Rev
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CHANNEL B: 2G/4G GDDR5

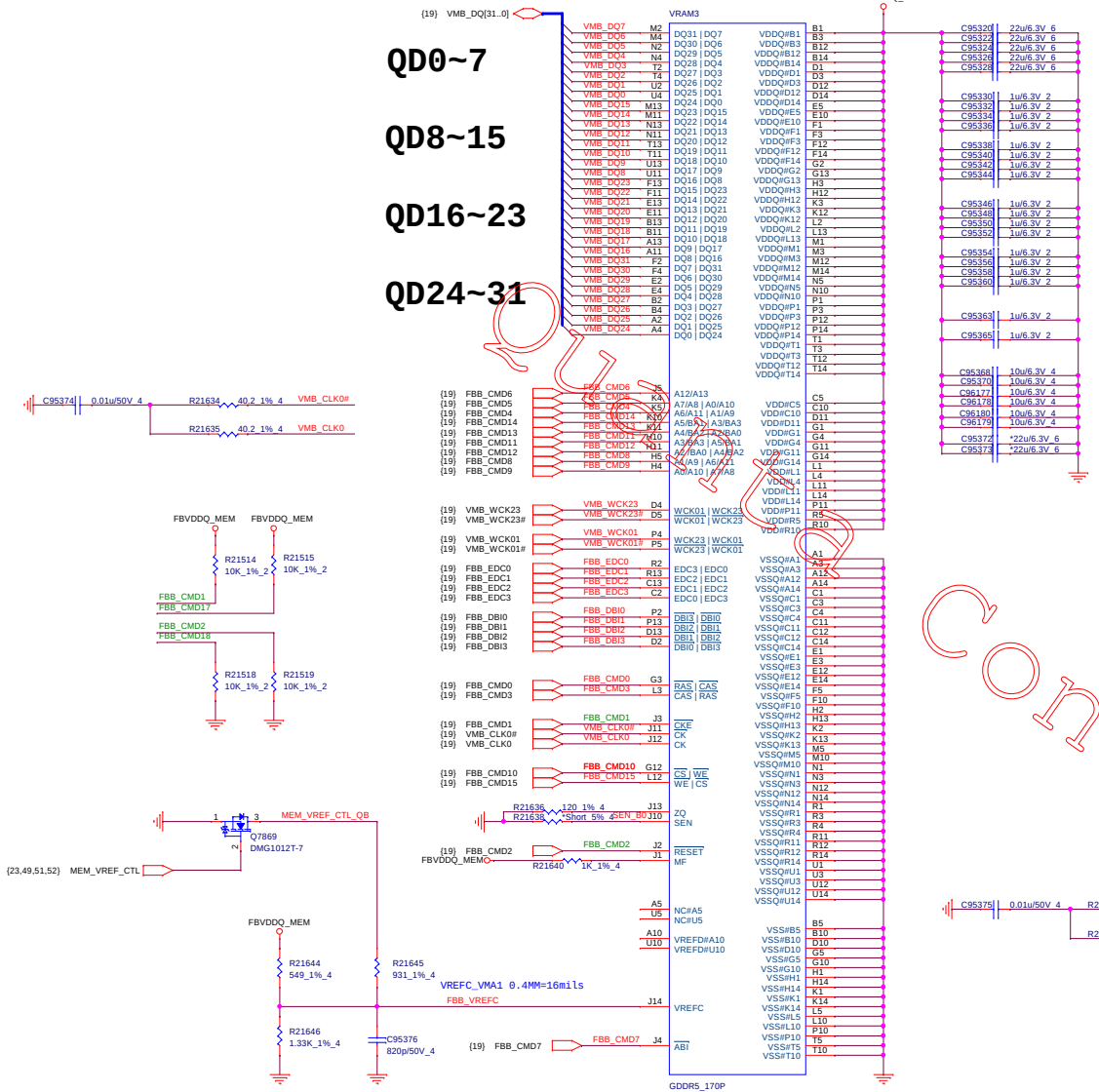
Channel 0 <0-31>
MF=1 mirrored

QD0~7

QD8~15

QD16~23

QD24~31



Channel 1 <0-31>
MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39

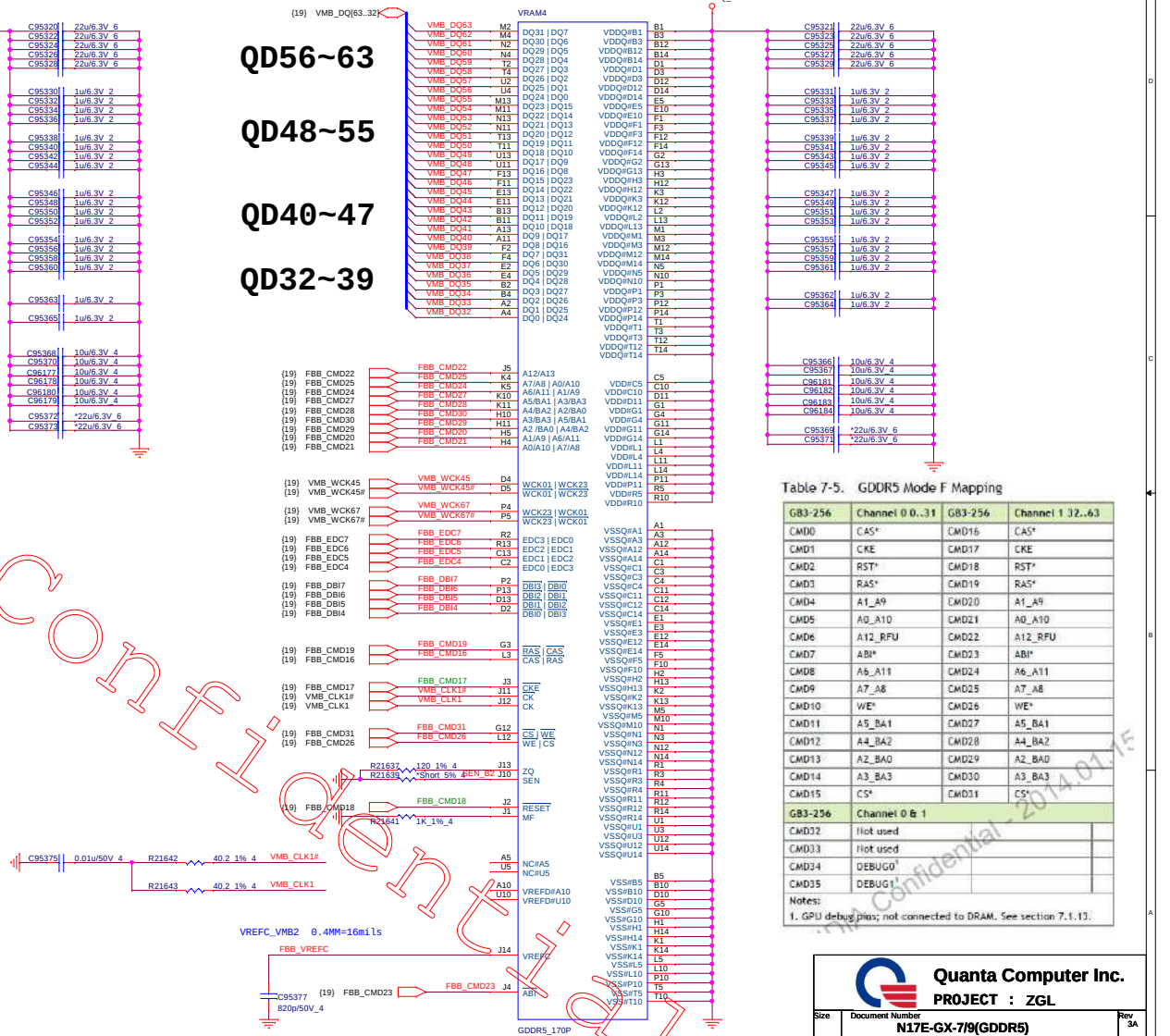


Table 7-5. GDDR5 Mode F Mapping

G83-256	Channel 0 0..31	G83-256	Channel 1 32..63
CMD0	CA5*	CMD16	CA5*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RA5*	CMD19	RA5*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
G83-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	N17E-GX-7/9(GDDR5)	3A
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CHANNEL C: 2G/4G GDDR5

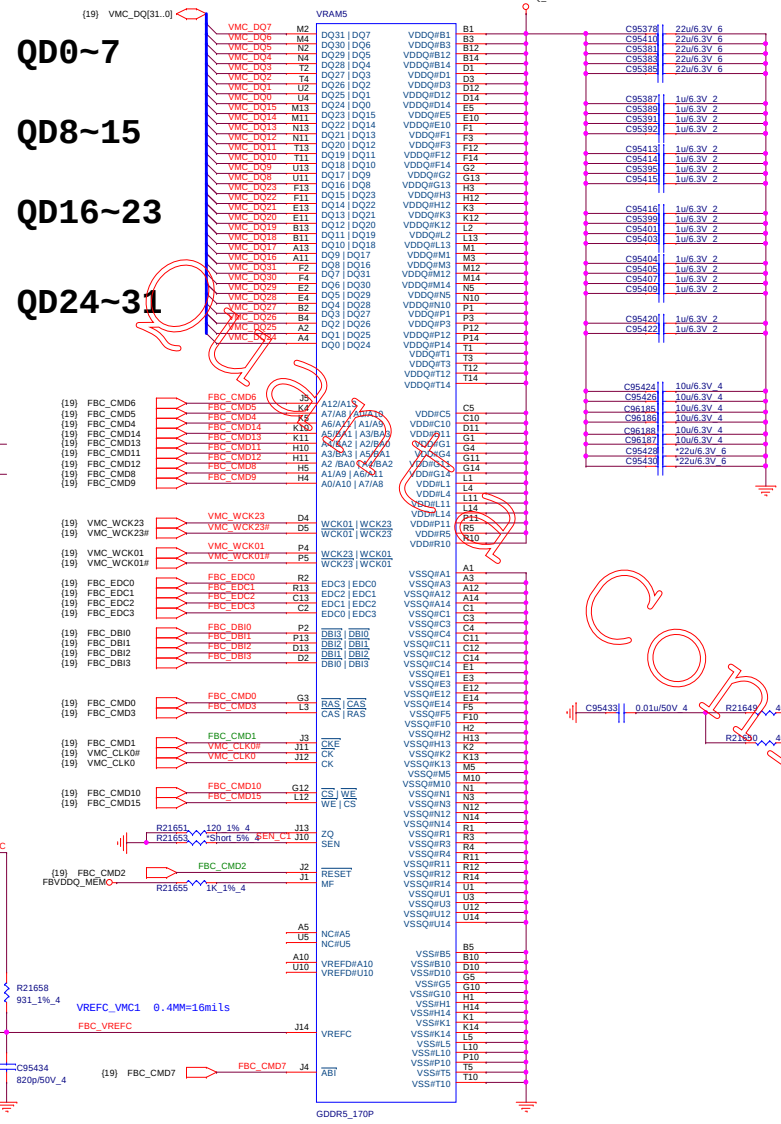
Channel 0 <0-31>
MF=0 Non-mirrored

QD0~7

QD8~15

QD16~23

QD24~31



Channel 1 <0-31>
MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39

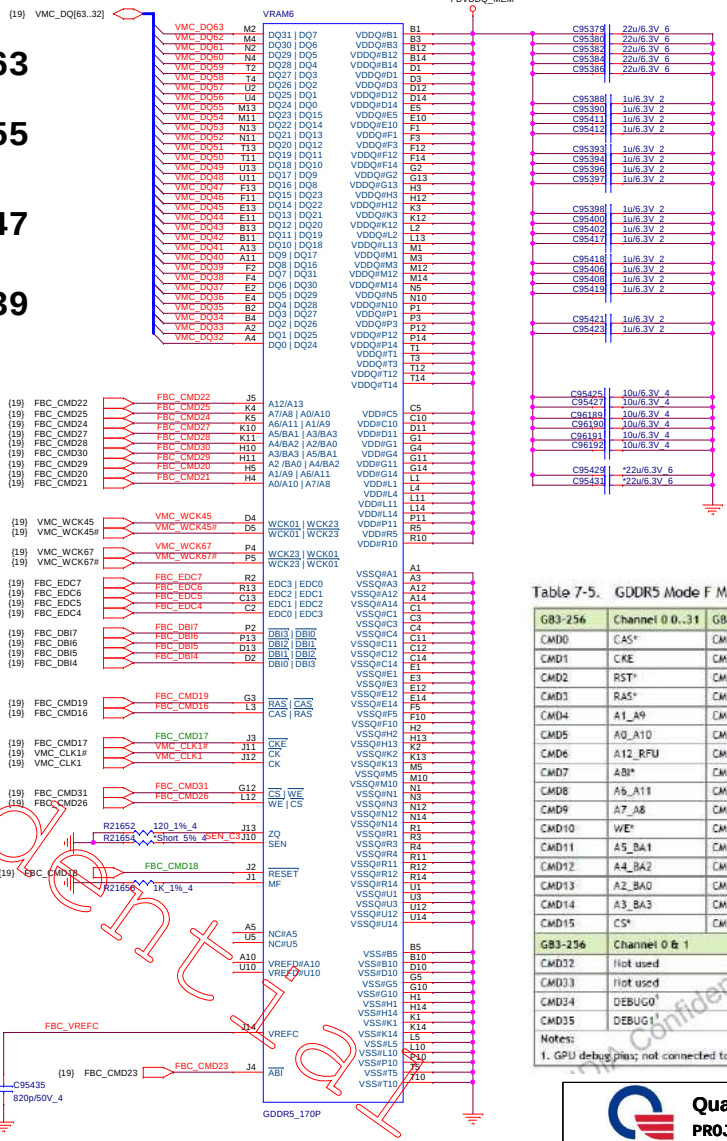


Table 7-5. GDDR5 Mode F Mapping

G83-256	Channel 0 0..31	G83-256	Channel 1 32..63
CMD0	CA5*	CMD16	CA5*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RA5*	CMD19	RA5*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
G83-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0*		
CMD35	DEBUG1*		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
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CHANNEL D: 2G/4G GDDR5

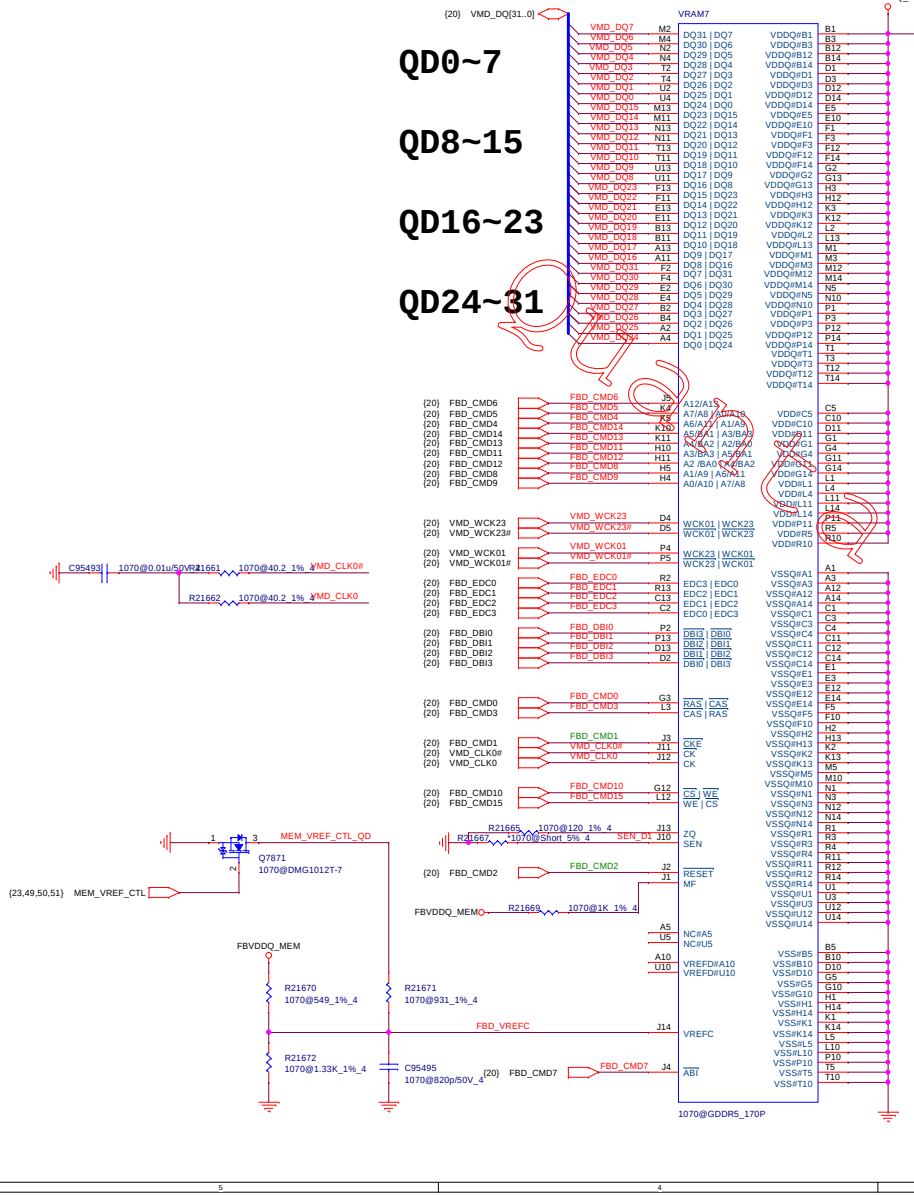
Channel 0 <0-31>
MF=1 mirrored

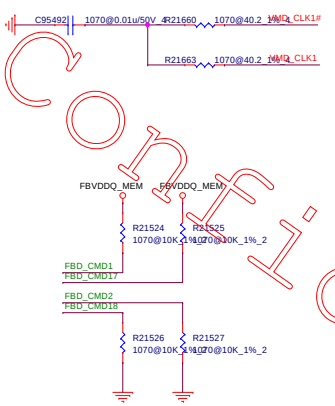
QD0~7

QD8~15

QD16~23

QD24~31





Channel 1 <0-31>
MF=0 Non-mirrored

QD56~63

QD48~55

QD40~47

QD32~39

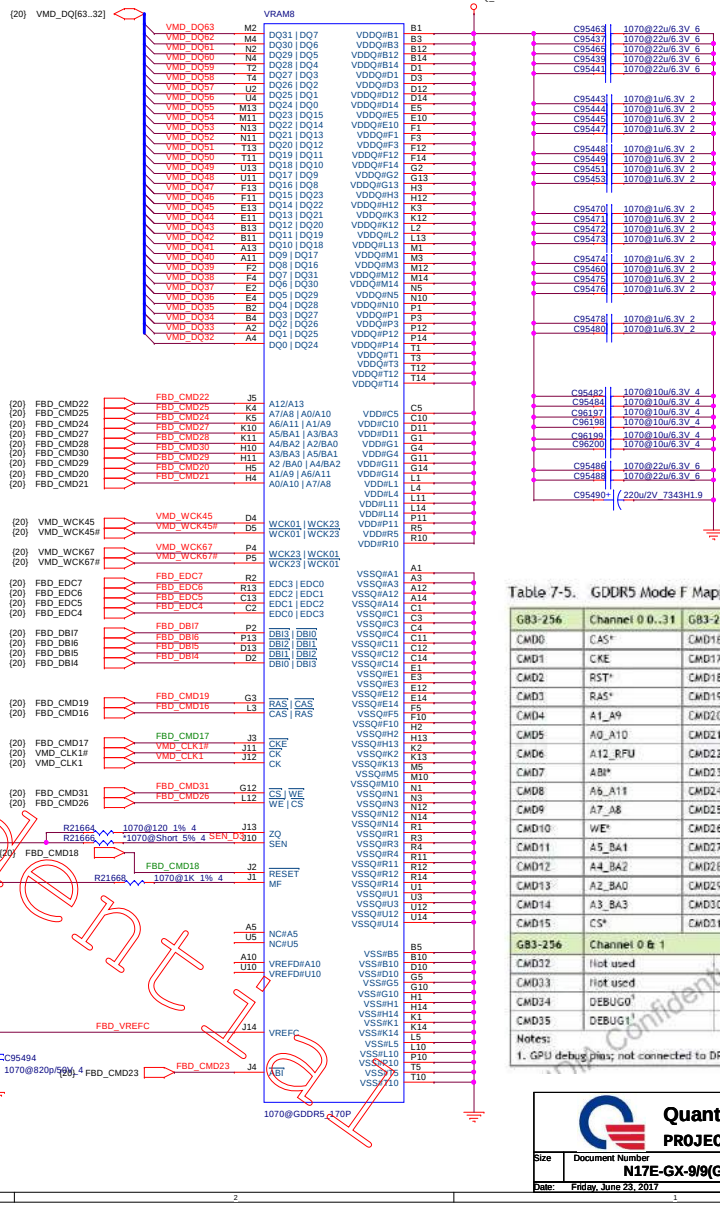


Table 7-5. GDDR5 Mode F Mapping

G83-256	Channel 0 0..31	G83-256	Channel 1 32..63
CMD0	CA5*	CMD16	CA5*
CMD1	CKE	CMD17	CKE
CMD2	RST*	CMD18	RST*
CMD3	RA5*	CMD19	RA5*
CMD4	A1_A9	CMD20	A1_A9
CMD5	A0_A10	CMD21	A0_A10
CMD6	A12_RFU	CMD22	A12_RFU
CMD7	ABI*	CMD23	ABI*
CMD8	A6_A11	CMD24	A6_A11
CMD9	A7_A8	CMD25	A7_A8
CMD10	WE*	CMD26	WE*
CMD11	A5_BA1	CMD27	A5_BA1
CMD12	A4_BA2	CMD28	A4_BA2
CMD13	A2_BA0	CMD29	A2_BA0
CMD14	A3_BA3	CMD30	A3_BA3
CMD15	CS*	CMD31	CS*
GB3-256	Channel 0 & 1		
CMD32	Not used		
CMD33	Not used		
CMD34	DEBUG0[1]		
CMD35	DEBUG1[1]		

Notes:
1. GPU debug pins; not connected to DRAM. See section 7.1.13.

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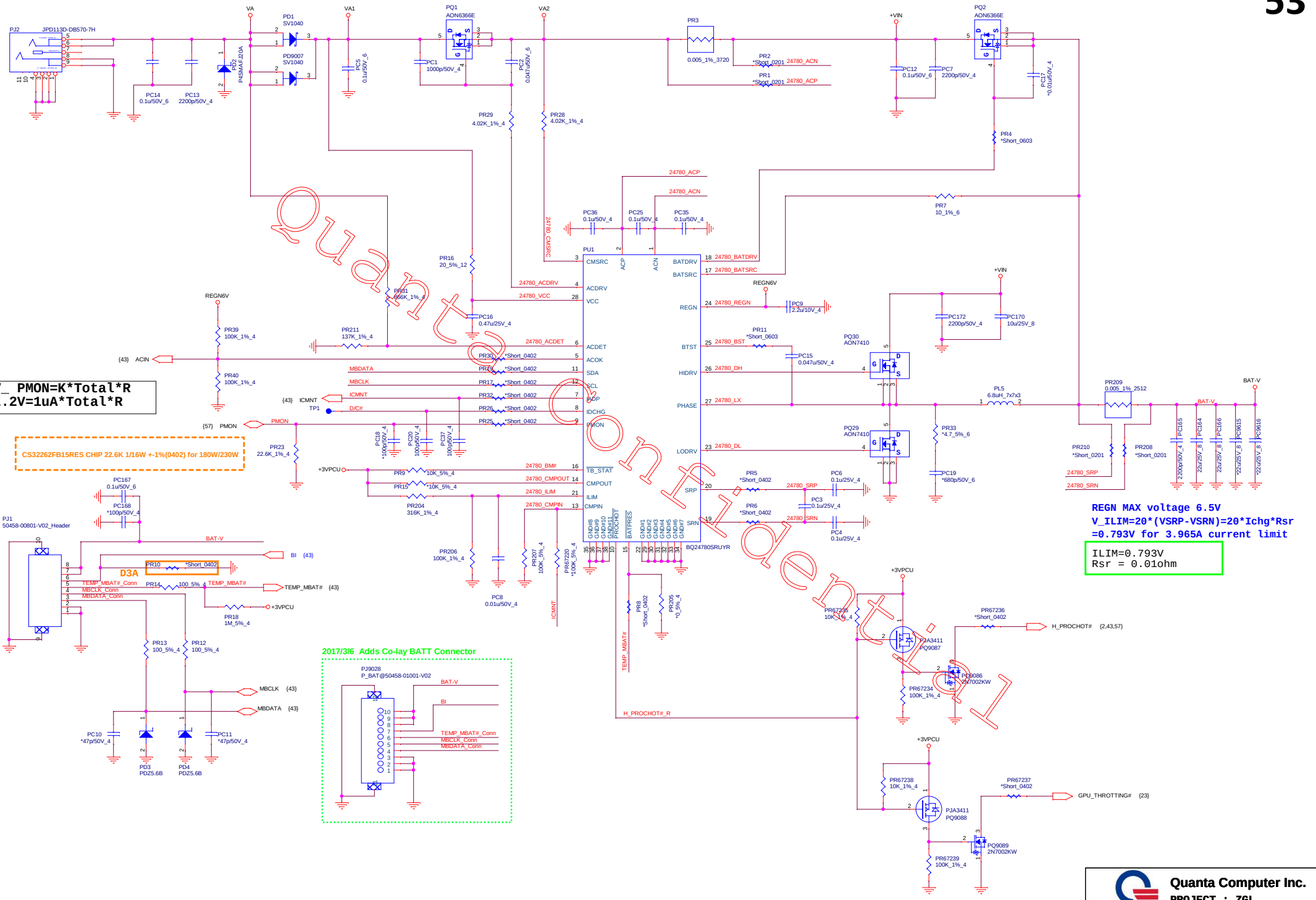
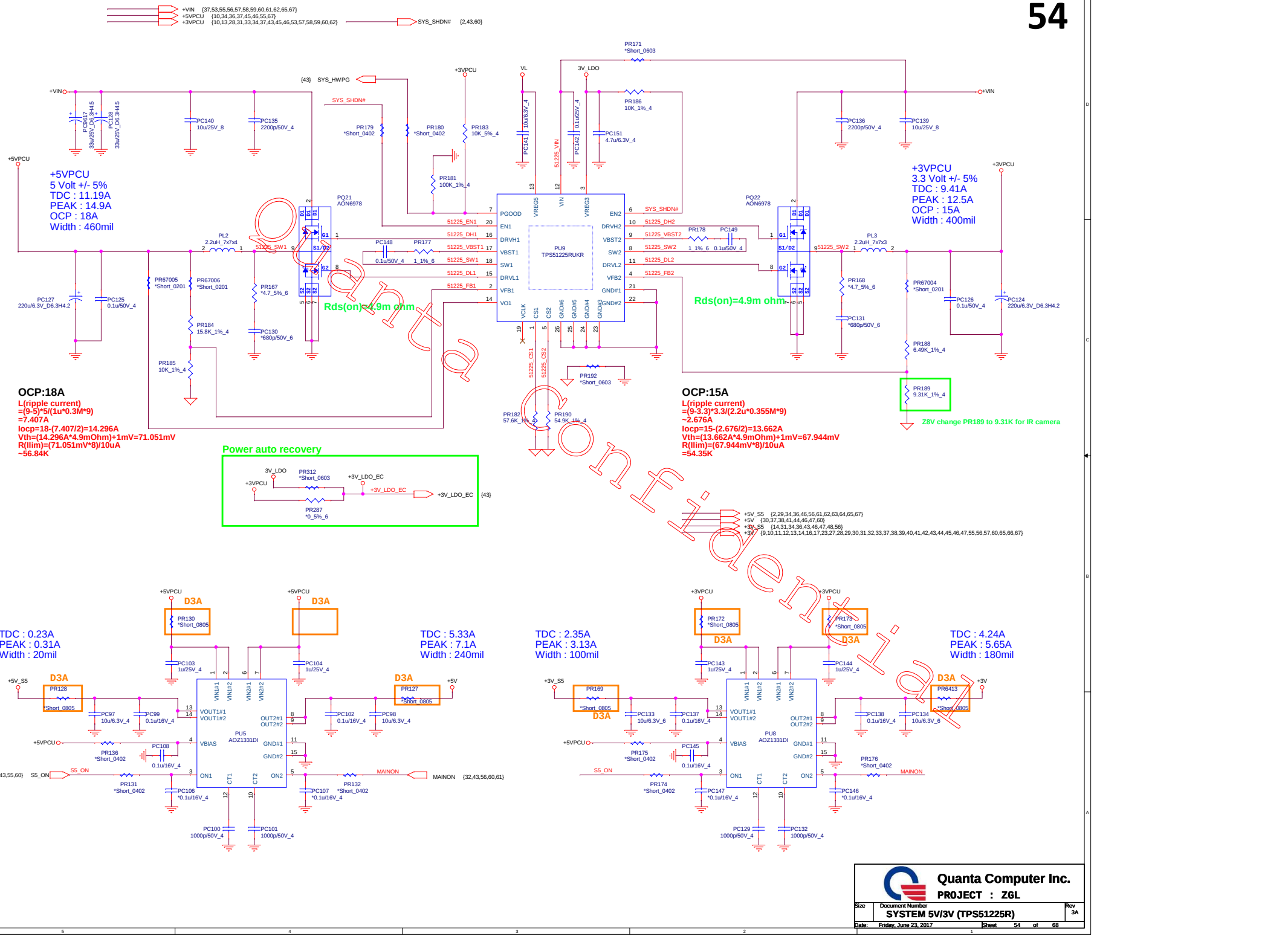
Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	N17E-GX-9/9(GDDR5)	3A

Date: Friday, June 23, 2017 Sheet 52 of 68


V_ PMON=K*Total*R
1.2V=1uA*Total*R
CS32262FB15RES CHIP 22.6K 1/16W +-1%(0402) for 180W/230W
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
ILIM=0.793V
Rsr = 0.01ohm
2017/3/6 Adds Co-lay BATT Connector
BQ24780SRUYR
PJ2 JPD113D-DB570-7H
PJ1 50458-00801-V02_Header
PJ9028 P_BAT@50458-01001-V02
D3A
PD1 SV1040
PD9007 SV1040
PD3 PDZ5.6B
PD4 PDZ5.6B
PQ1 AON6366E
PQ2 AON6366E
PQ30 AON7410
PQ29 AON7410
PJA3411 PQ9087
PQ9086 2N7002KW
PJA3411 PQ9088
PQ9089 2N7002KW
PU1
VA
VA1
VA2
+VIN
REGN6V
BAT-V
TP1
PR3 0.005_1%_3720
PR4 *Short_0603
PR7 10_1%_6
PR16 20_5%_12
PR23 22.6K_1%_4
PR39 100K_1%_4
PR40 100K_1%_4
PR211 137K_1%_4
PR231 866K_1%_4
PR204 316K_1%_4
PR206 100K_1%_4
PR207 100K_5%_4
PR67220 *100K_5%_4
PR67236 10K_1%_4
PR67238 10K_1%_4
PR67234 100K_1%_4
PR67239 100K_1%_4
PR67236 *Short_0402
PR67237 *Short_0402
PR67238 *Short_0402
PR209 0.005_1%_2512
PR210 *Short_0201
PR208 *Short_0201
PR33 *4.7_5%_6
PR11 *Short_0603
PL5 6.8uH_7x7x3
PC1 1000p/50V_4
PC2 0.047u/50V_6
PC5 0.1u/50V_6
PC7 2200p/50V_4
PC8 0.01u/50V_4
PC9 2.2u/10V_4
PC10 *47p/50V_4
PC11 *47p/50V_4
PC12 0.1u/50V_6
PC13 2200p/50V_4
PC14 0.1u/50V_6
PC15 0.047u/50V_4
PC16 0.47u/25V_4
PC17 *0.01u/50V_4
PC19 *680p/50V_6
PC25 0.1u/50V_4
PC35 0.1u/50V_4
PC36 0.1u/50V_4
PC167 0.1u/50V_6
PC168 *100p/50V_4
PC170 10u/25V_8
PC172 2200p/50V_4
PC3 0.1u/25V_4
PC4 0.1u/25V_4
PC6 0.1u/25V_4
PC18 *100p/50V_4
PC20 100p/50V_4
PC37 100p/50V_4
PC165 2200p/50V_4
PC164 22u/25V_8
PC166 22u/25V_8
PC9615 *22u/25V_8
PC9616 *22u/25V_8
PR5 *Short_0402
PR6 *Short_0402
PR8 *Short_0402
PR10 *Short_0402
PR205 *0_5%_4
PR12 100_5%_4
PR13 100_5%_4
PR14 100_5%_4
PR18 1M_5%_4
PR25 *Short_0402
PR26 *Short_0402
PR27 *Short_0402
PR30 *Short_0402
PR32 *Short_0402
PR9 10K_5%_4
PR15 *10K_5%_4
PR2 *Short_0201 24780_ACN
PR1 *Short_0201 24780_ACP
24780_ACP
24780_ACN
24780_CMSRC
24780_ACDRV
24780_VCC
24780_ACDET
24780_BATDRV
24780_BATSRC
24780_REGN
24780_BST
24780_DH
24780_LX
24780_DL
24780_SRP
24780_SRN
24780_BM#
24780_CMPOUT
24780_ILIM
24780_CMPIN
ACIN
ICMNT
PMON
MBDATA
MBCLK
D/C#
TEMP_MBAT#
TEMP_MBAT#_Conn
MBCLK_Conn
MBDATA_Conn
H_PROCHOT#
H_PROCHOT#_R
GPU_THROTTING#
BI
CMSRC
ACDRV
VCC
ACDET
ACOK
SDA
SCL
ICOP
IDCHG
PMON
TB_STAT
CMPOUT
ILIM
CMPIN
BATDRV
BATSRC
REGN
BTST
HIDRV
PHASE
LODRV
SRP
SRN
BATPRES
PROCHOT
ACP
ACN
Quanta Computer Inc.
PROJECT : ZGL
Charger (BQ24780S)
Size
Document Number
Rev
3A
Date: Friday, June 23, 2017
Sheet 53 of 68


+VIN {37,53,55,56,57,58,59,60,61,62,65,67}
+5VPCU {10,34,36,37,45,46,55,67}
+3VPCU {10,13,28,31,33,34,37,43,45,46,53,57,58,59,60,62}
SYS_SHDN# {2,43,60}
+5VPCU
5 Volt +/- 5%
TDC : 11.19A
PEAK : 14.9A
OCP : 18A
Width : 460mil
+3VPCU
3.3 Volt +/- 5%
TDC : 9.41A
PEAK : 12.5A
OCP : 15A
Width : 400mil
PU9 TPS51225RUKR
PQ21 AON6978
PQ22 AON6978
Rds(on)=4.9m ohm
OCP:18A
L(ripple current)
=(9-5)*5/(1u*0.3M*9)
=7.407A
Iocp=18-(7.407/2)=14.296A
Vth=(14.296A*4.9mOhm)+1mV=71.051mV
R(Ilim)=(71.051mV*8)/10uA
~56.84K
OCP:15A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.355M*9)
~2.676A
Iocp=15-(2.676/2)=13.662A
Vth=(13.662A*4.9mOhm)+1mV=67.944mV
R(Ilim)=(67.944mV*8)/10uA
=54.35K
Z8V change PR189 to 9.31K for IR camera
Power auto recovery
+5V_S5 {2,29,34,36,46,56,61,62,63,64,65,67}
+5V {30,37,38,41,44,46,47,60}
+3V_S5 {14,31,34,36,43,46,47,48,56}
+3V {9,10,11,12,13,14,16,17,23,27,28,29,30,31,32,33,37,38,39,40,41,42,43,44,45,46,47,55,56,57,60,65,66,67}
TDC : 0.23A
PEAK : 0.31A
Width : 20mil
TDC : 5.33A
PEAK : 7.1A
Width : 240mil
TDC : 2.35A
PEAK : 3.13A
Width : 100mil
TDC : 4.24A
PEAK : 5.65A
Width : 180mil
PU5 AOZ1331DI
PU8 AOZ1331DI
MAINON {32,43,56,60,61}
{43,55,60} S5_ON
{43} SYS_HWPG
+3V_LDO_EC {43}
Quanta Computer Inc.
PROJECT : ZGL
SYSTEM 5V/3V (TPS51225R)
Rev 3A
Friday, June 23, 2017
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+VIN {37,53,54,56,57,58,59,60,61,62,65,67}
+1V_S5 {10,11,14}
+5VPCU {10,34,36,37,45,46,54,67}
+3V {9,10,11,12,13,14,16,17,23,27,28,29,30,31,32,33,37,38,39,40,41,42,43,44,45,46,47,54,56,57,60,65,66,67}
+1V_SUS {2,6,10,57}
+VCCIO {2,3,6,10,23,57,60}

D3A
PJ3004
*short3720
+1V_S5_VIN
+VIN
PC220
2200p/50V_6
PC221
10u/25V_8
+5VPCU
PC223
1u/10V_4
+3V
PR263
100K_1%_4
PU9015
RT8237CZQW_2
PQ9053
AON6978
{43} HWPG_1VS5
{43,54,60} S5_ON
{43} +1V_S5_ON
PR266
*Short_0402
PR115
*0_5%_4
PR114
*100K_1%_4
PR265
42.2K_1%_4
PR268
470K_1%_4
51211V_EN
51211V_TRIP
51211V_TST
PGOOD
EN
CS
RF
VCC
FB
UGATE
BOOT
PHASE
LGATE
GND#1
51211V_DRVH
51211V_VBST
51211V_SW
51211V_DRVL
D3A
PC222
0.1u/50V_6
PR264
*Short_0603
PL12
0.68uH_7x7x3
+1V_S5_SRC
D3A
PJ3005
*short3720
+1V_S5
PR112
*4.7_5%_6
PC81
*680p/50V_6
PR67007
*Short_0201
PC217
0.1u/50V_6
PC219
330u/2V_7343H1.9
Check EN sequence with HW
OCP=13A
L ripple current
=(19-1)*1/(0.68u*290k*19)
=4.804A
Vtrip=13-(4.804/2)*4.9mohm
=51.9302mV
Rlimit=51.9302mV/10uA*8=41.54Kohm
RDSon=4.9mohm
PR67003
4.3K_1%_4
PR267
10K_1%_4
VFB=0.7V
+1V_S5
1.0 Volt +/- 5%
TDC : 8.19A
PEAK : 10.92A
OCP : 13A
Width : 340mil
+VIN
+1V_SUS
+VIN
+1V_S5
PR84
1M_5%_6
PR86
22_5%_8
PR66972
1M_5%_6
PR83
1M_5%_6
{34,43,56,61} SUSON
PQ8
LTC044EUBFS8TL
PQ9059
2N7002K
PQ9054
2N7002K
PC62
*2200p/50V_4
SUSD
PR255
*0_5%_6
PQ9055
PJA3404
+1V_SUS
{56,60} MAIND
MAIND
PQ9056
TPCA8064-H
+VCCIO
TDC : 0.23A
PEAK : 0.31A
Width : 20mil
TDC : 4.13A
PEAK : 5.5A
Width : 180mil

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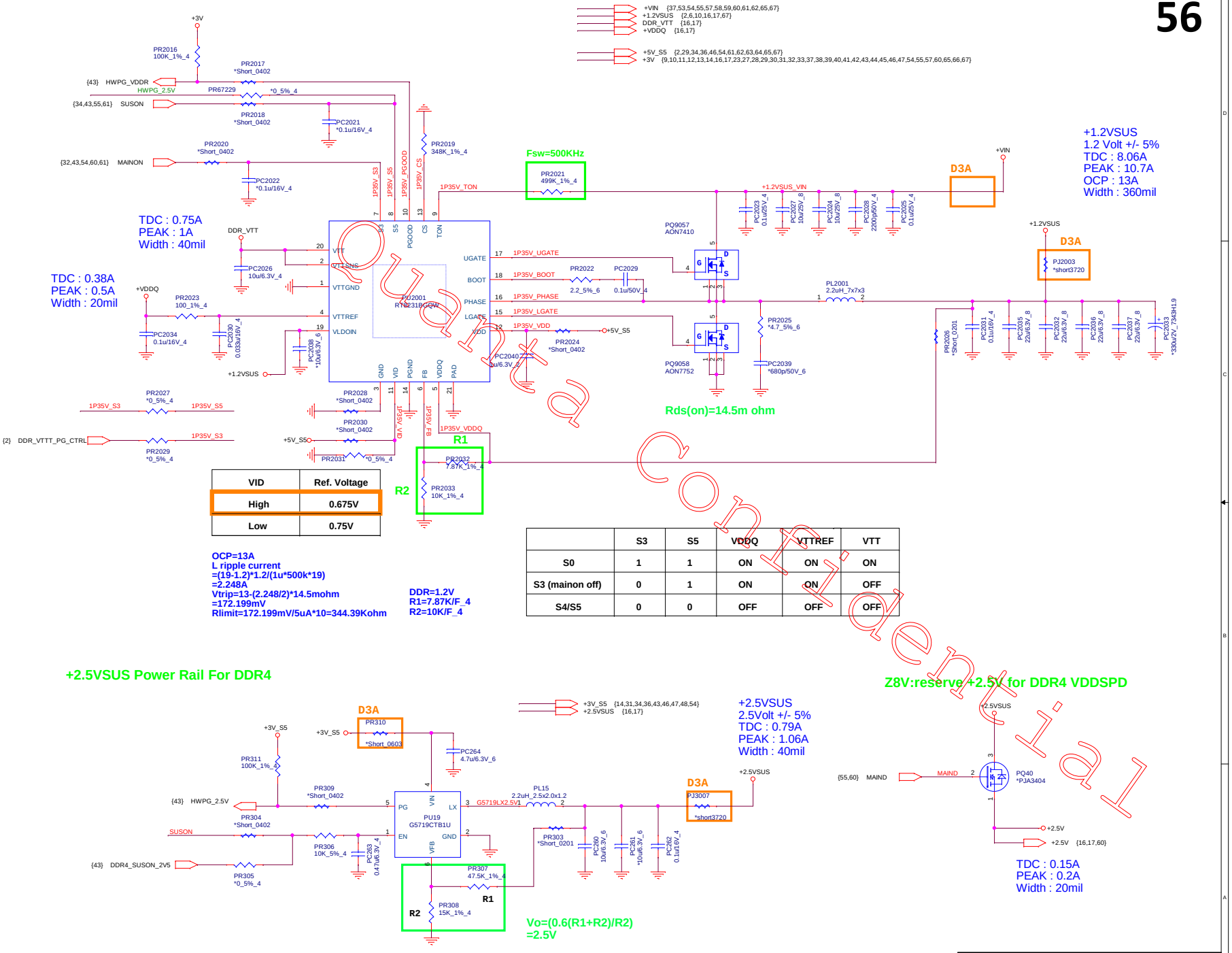
Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: +1V_S5 (RT8237CZQW_2)	Rev: 3A
Date: Friday, June 23, 2017	Sheet 55 of 68	



VID	Ref. Voltage
High	0.675V
Low	0.75V

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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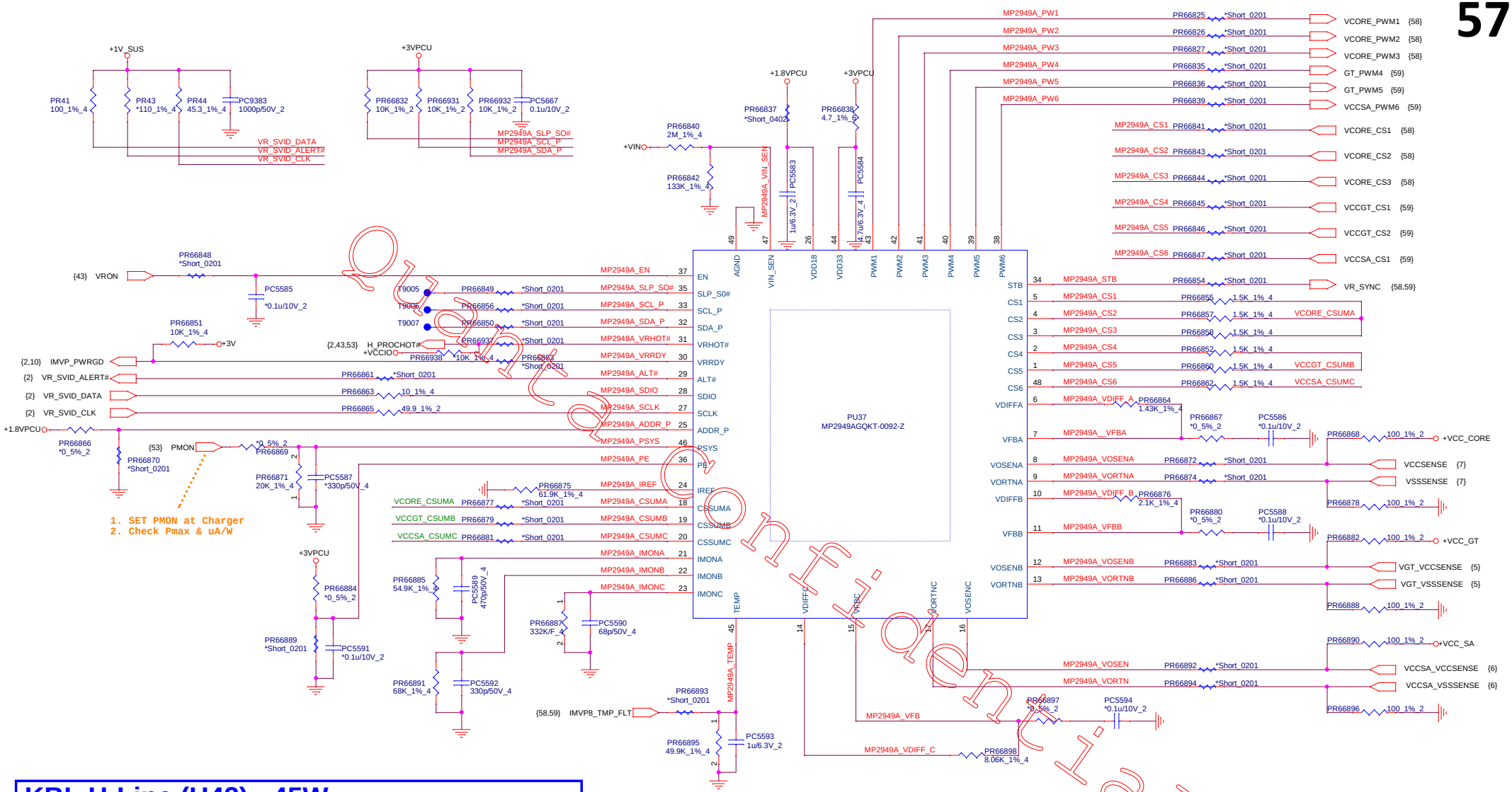
Quanta Computer Inc.			
PROJECT : ZGL			
Size	Document Number		Rev
	DDR4_+1.2VSUS (RT8231BGQW)		3A
Date: Friday, June 23, 2017	Sheet 56 of 68		



KBL H-Line (H42) - 45W (3+2+1 Phase)

Vcore	VCCGT	VCCSA
Icc TDC：50A	Icc TDC：25A	Icc TDC：10A
Icc Max：68A	Icc Max：55A	Icc Max：11.1A
OCP：92A	OCP：75A	OCP：16A
VCORE L/L：	**VCORE L/L：**	**VCORE L/L：**
R_DC_LL：1.8mV/A	R_DC_LL：2.65mV/A	R_DC_LL：10mV/A
R_AC_LL：1.8mV/A	R_AC_LL：2.65mV/A	R_AC_LL：10mV/A

+VIN {37,53,54,55,56,58,59,60,61,62,65,67}
+VCC_CORE {7,58}
+VCC_GT {5,7,59}
+VCC_SA {6,59}
+3VPCU {10,13,28,31,33,34,37,43,45,46,53,54,58,59,60,62}
+3V {9,10,11,12,13,14,16,17,23,27,28,29,30,31,32,33,37,38,39,40,41,42,43,44,45,46,47,54,55,56,60,65,66,67}
+1V_SUS {2,6,10,55}
+VCCIO {2,3,6,10,23,55,60}

Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	CPU VR IC (MP2949A)	3A
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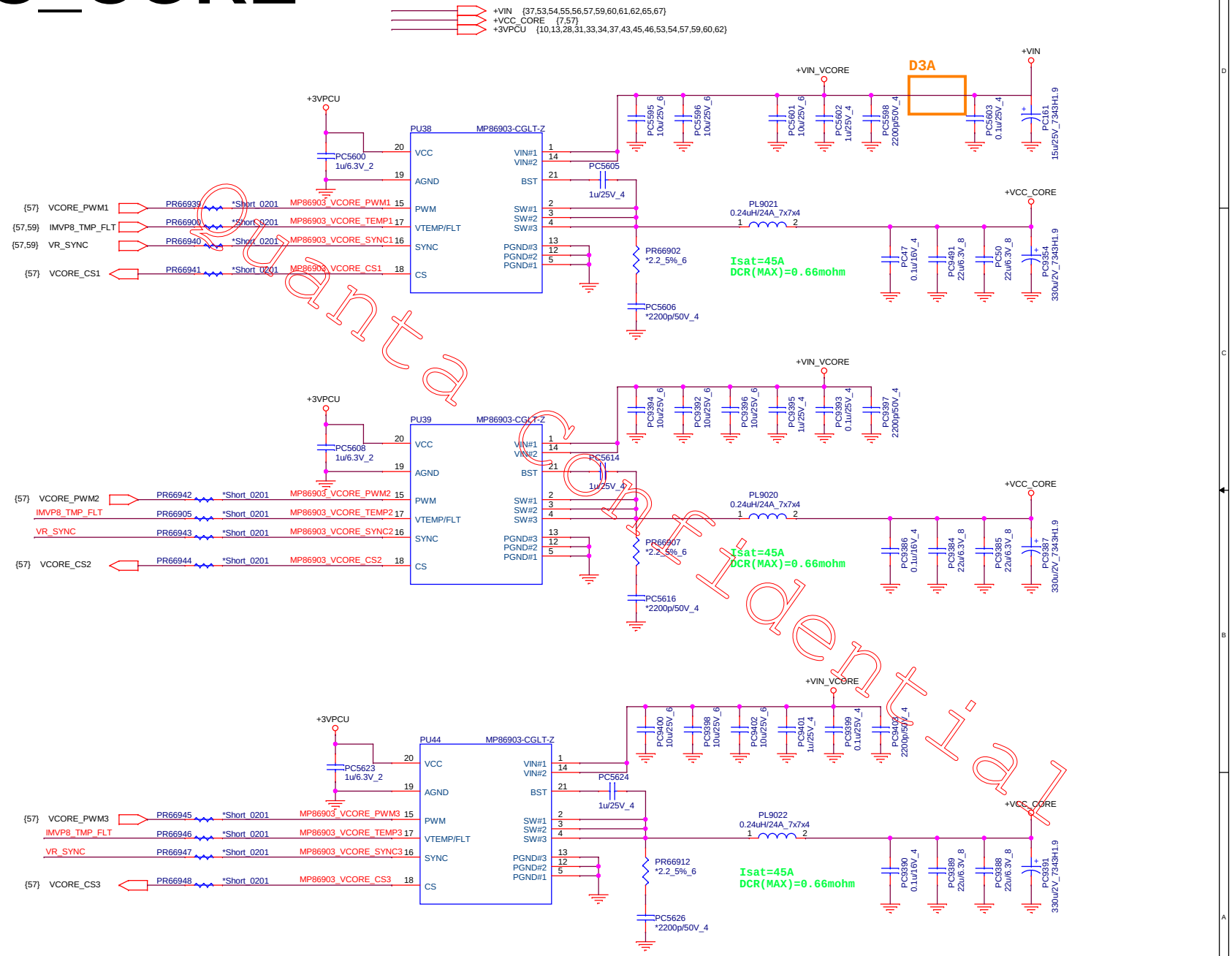
+VCC_CORE



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Quanta Computer Inc.

PROJECT : ZGL

Size	Document Number	Rev
	+VCC_CORE (MP86903)	3A

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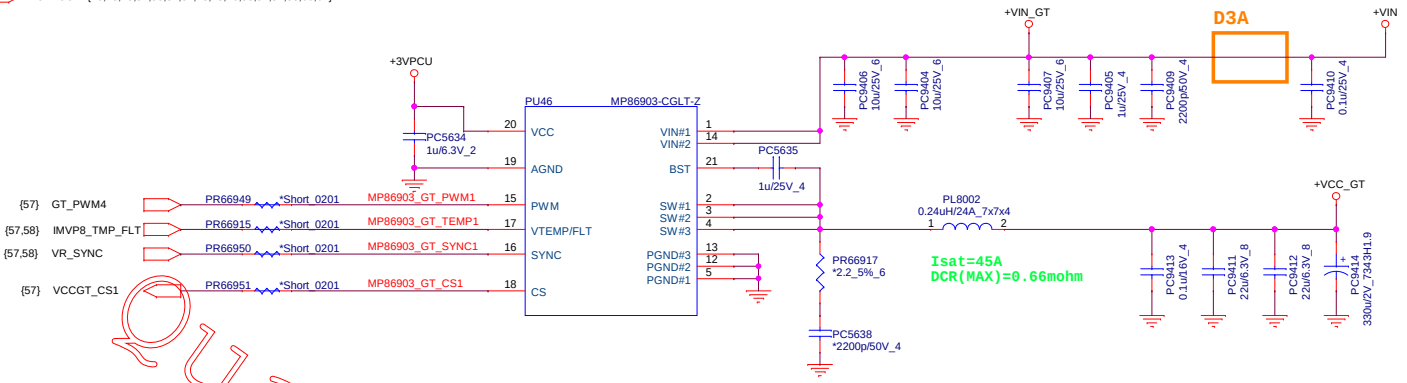
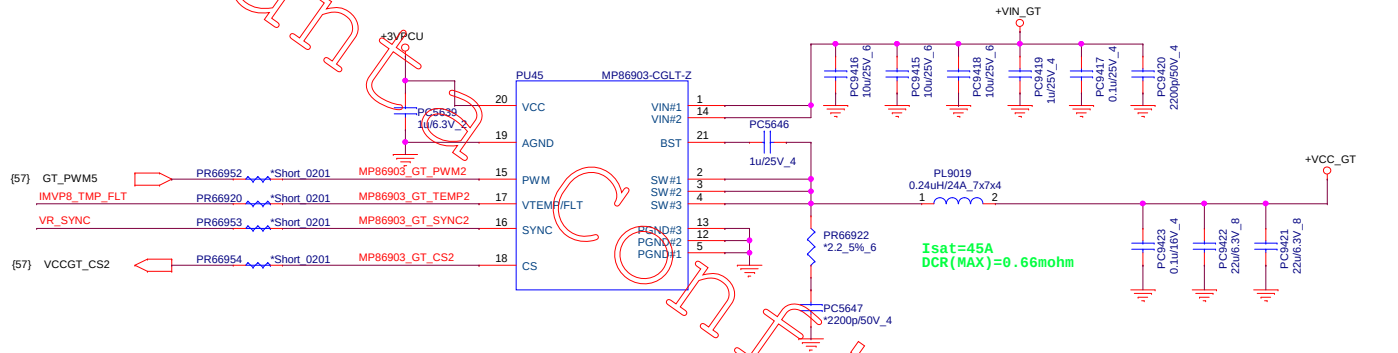
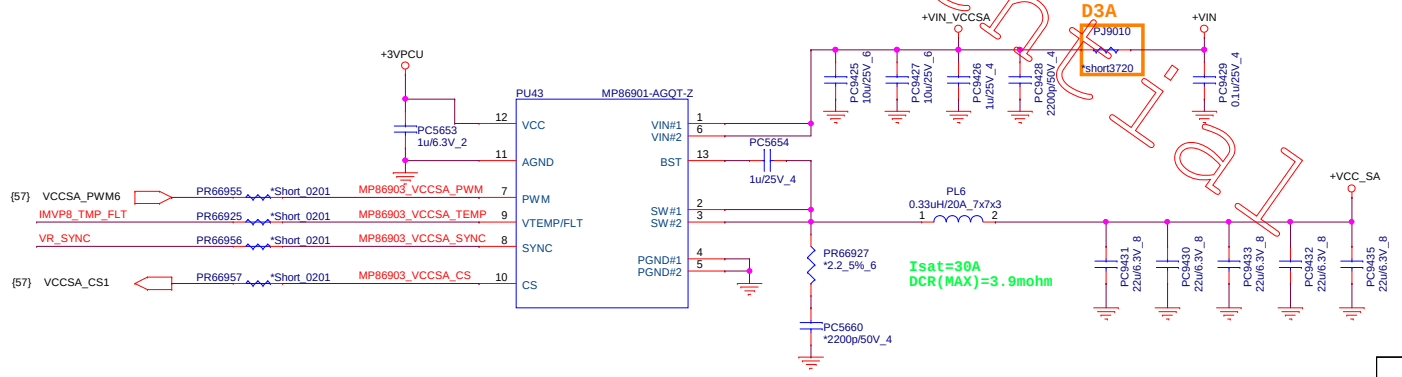
GT

+VIN {37,53,54,55,56,57,58,60,61,62,65,67}
+VCC_GT {5,7,57}
+VCC_SA {6,57}
+3VPCU {10,13,28,31,33,34,37,43,45,46,53,54,57,58,60,62}





VCCSA



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Quanta Computer Inc.		
PROJECT : Z6L		
Size	Document Number: +VCCGT/SA (MP86901)	Rev: 3A
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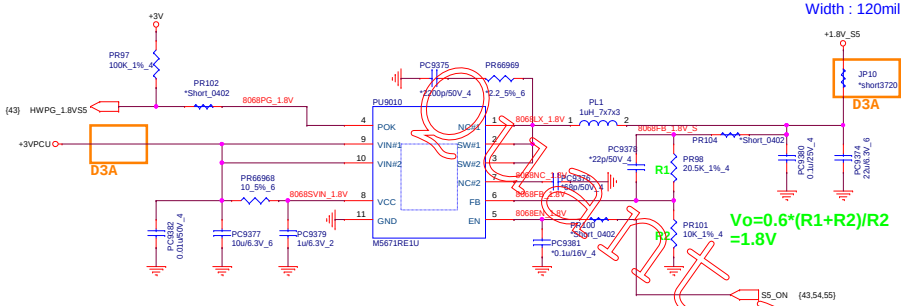
+3VPCU {10,13,28,31,33,34,37,43,45,46,53,54,57,58,59,62}
+1.8V_S5 {67}
+1.8V {24,28,37,38}
+3V_S5 {14,31,34,36,43,46,47,48,54,56}
+3V {9,10,11,12,13,14,16,17,23,27,28,29,30,31,32,33,37,38,39,40,41,42,43,44,45,46,47,54,55,56,57,65,66,67}

+VIN {37,53,54,55,56,57,58,59,61,62,65,67}
+5V {30,37,38,41,44,46,47,54}
+VCCIO {2,3,6,10,23,55,57}
+2.5V {16,17,56}

+1.8V_S5
1.8Volt +/- 5%
TDC : 2.61A
PEAK : 3.48A
Width : 120mil

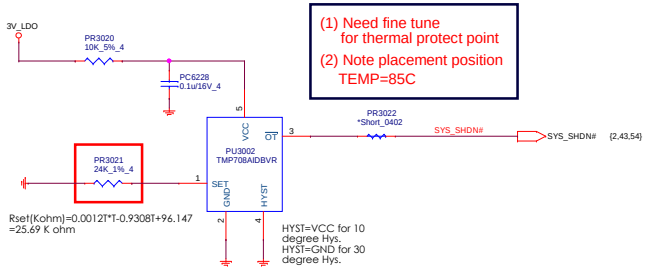


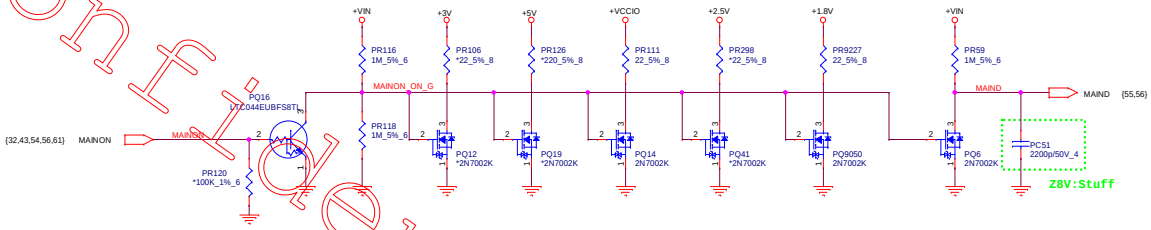
Vo=0.6*(R1+R2)/R2
=1.8V

TDC : 0.08A
PEAK : 0.1A
Width : 20mil

Thermal protection

(1) Need fine tune
for thermal protect point
(2) Note placement position
TEMP=85C





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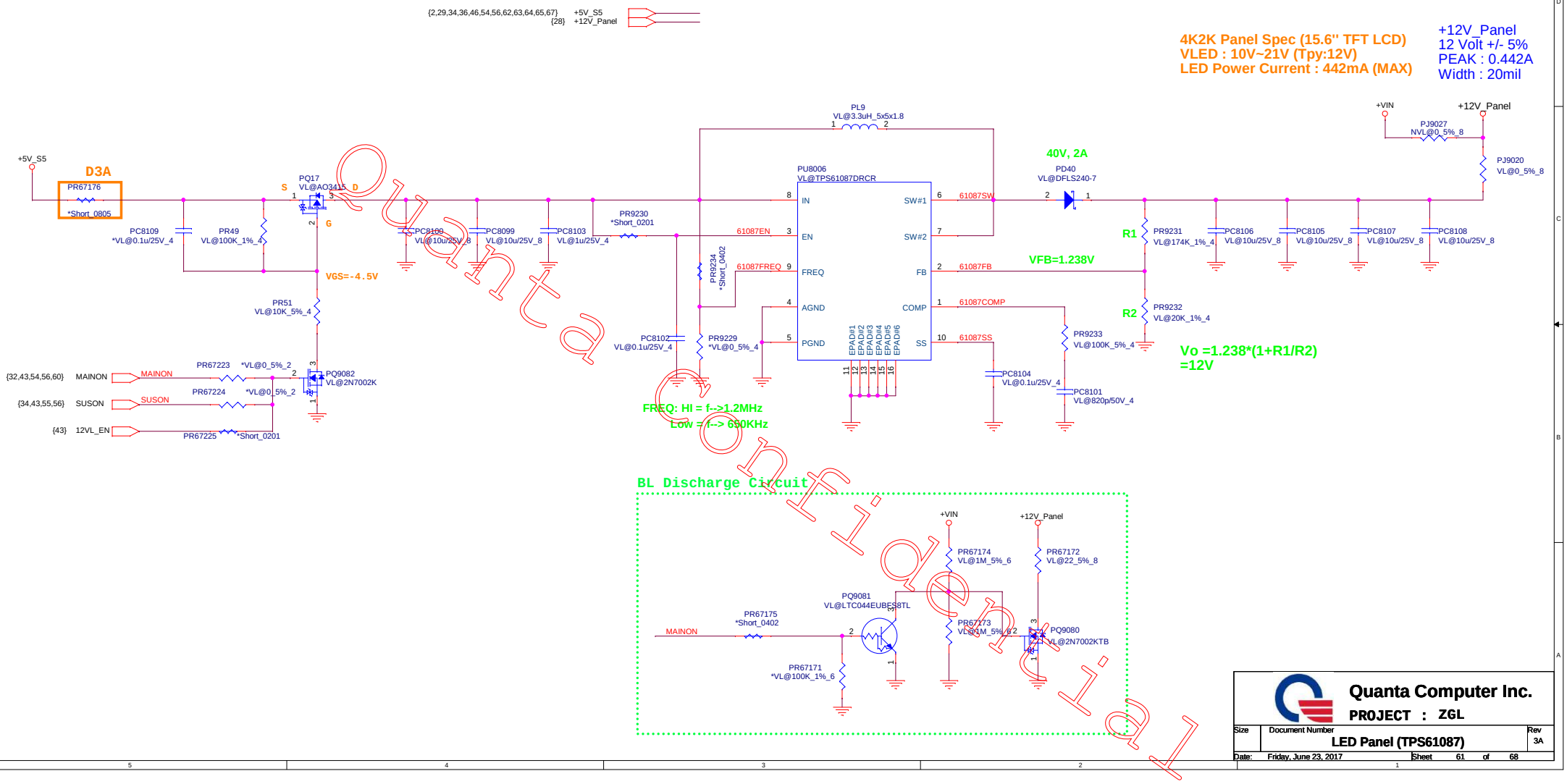
Quanta Computer Inc.		
PROJECT : ZGL		
Size	Document Number: +1.8V_S5/+1.5V/Thermal Protect	Rev 3A
Date: Friday, June 23, 2017	Sheet 60 of 68	

LED Panel (TPS61087)



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Quanta Computer Inc. PROJECT : ZGL		
Size	Document Number: LED Panel (TPS61087)	Rev: 3A
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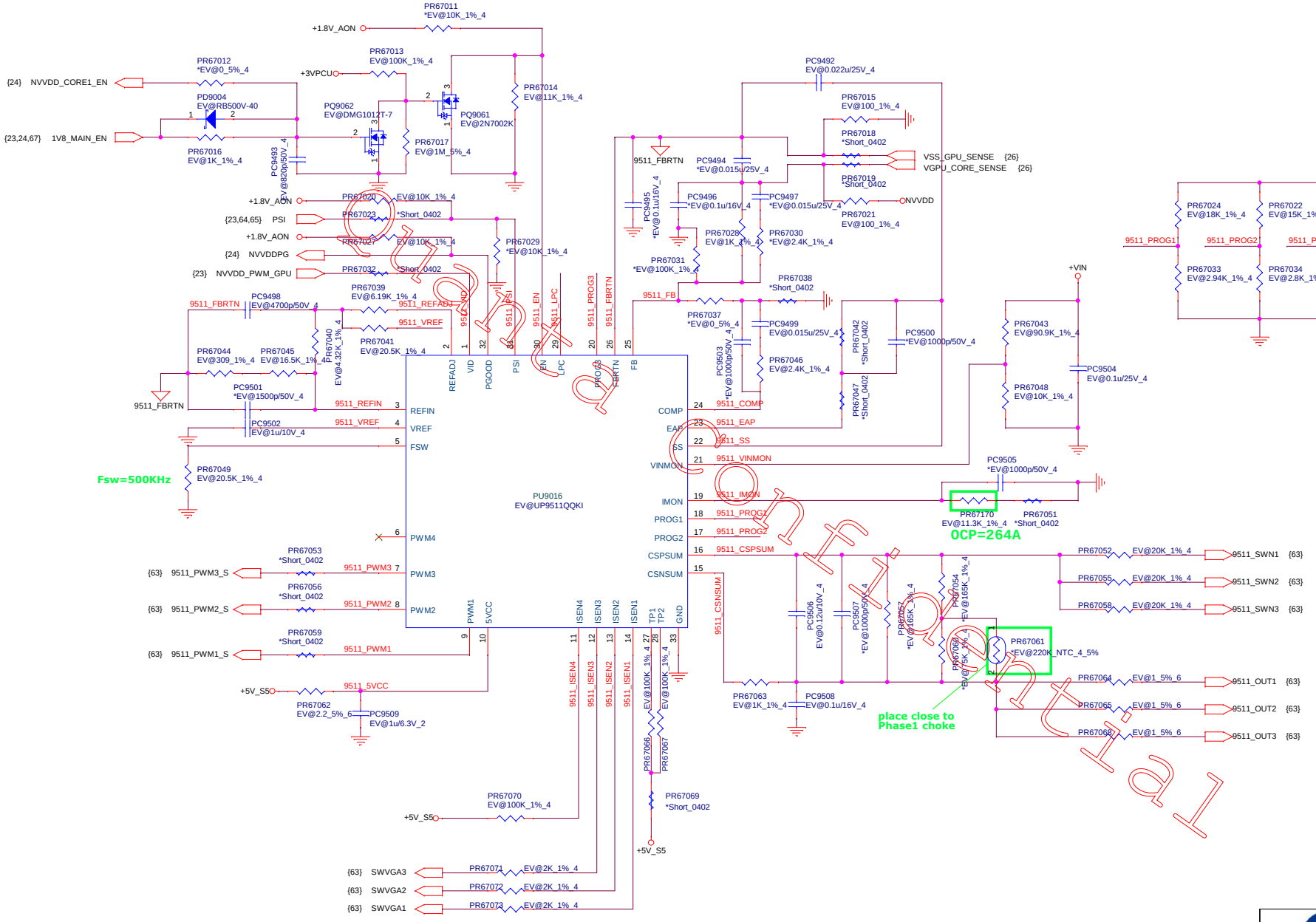
VGA Core - NVVDD/NVDDS

+VIN {37,53,54,55,56,57,58,59,60,61,65,67}
NVVDD {26,63}
+5V_S5 {2,29,34,36,46,54,56,61,63,64,65,67}
+1.8V_AON {18,21,22,23,24,25,64,65,67}



N17E-G2(115W)
1070 MAX P

NVVDD
EDP-Continous:85A
EDP-Peak:203A
OCP:264A

N17E-G2(90W)
1070 MAX Q

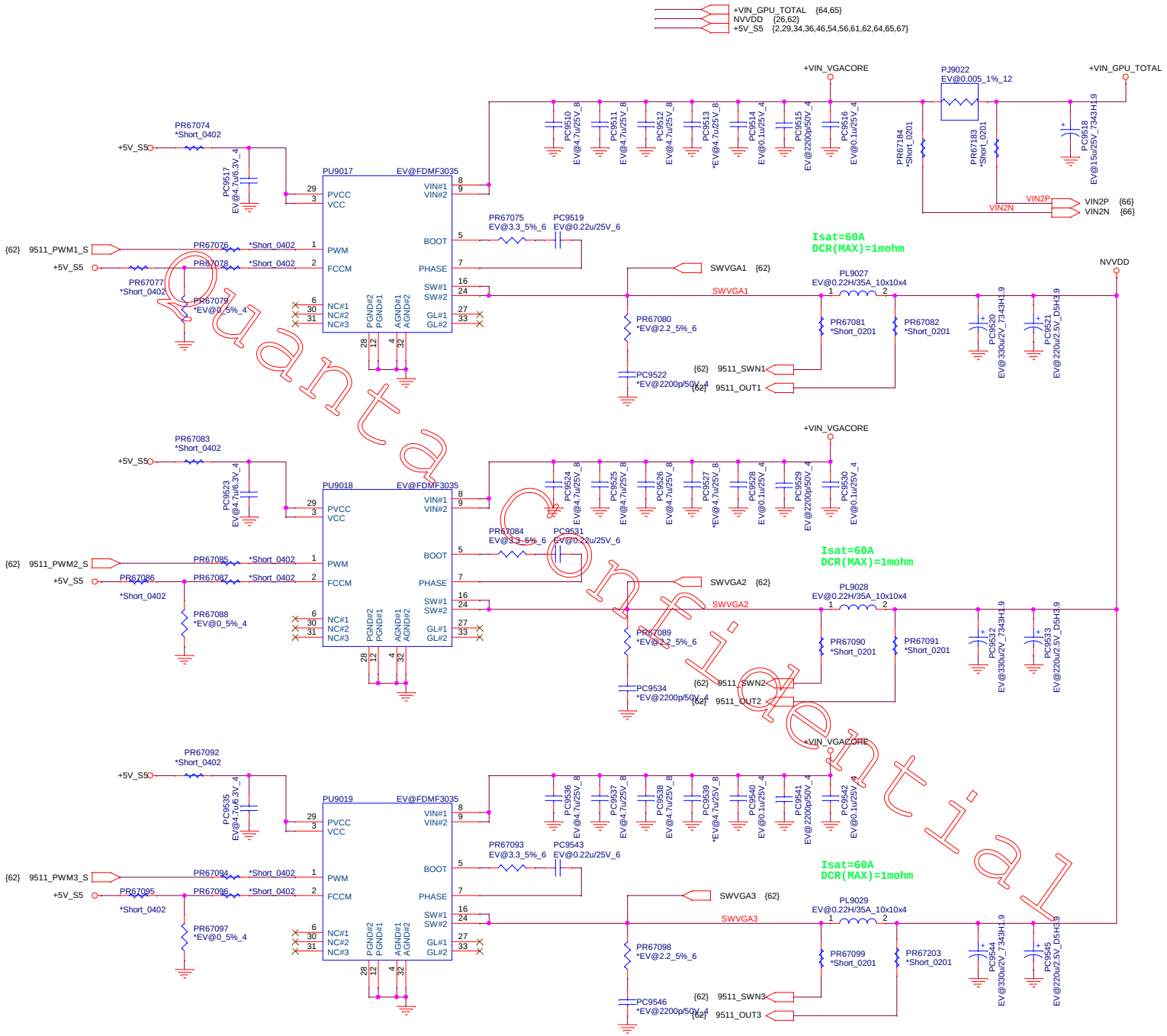
NVVDD
EDP-Continous:66.12A
EDP-Peak:142.55A
OCP:264A

N17E-G1(TGP78W)
1060 MAX P

NVVDD
EDP-Continous:60A
EDP-Peak:127A
OCP:264A

Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	+VGPU (uP9511QQKI)	3A
Date: Friday, June 23, 2017	Sheet 62 of 68	



N17E-G2(115W)
1070 MAX P
NVVDD EDP-Continous:85A EDP-Peak:203A OCP:264A

N17E-G2(90W)
1070 MAX Q
NVVDD EDP-Continous:66.12A EDP-Peak:142.55A OCP:264A

N17E-G1(TGP78W)
1060 MAX P
NVVDD EDP-Continous:60A EDP-Peak:127A OCP:264A

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Quanta Computer Inc.
PROJECT : ZGL

Size	Document Number	Rev
	+VGPU (uP9511QQKI)	3A
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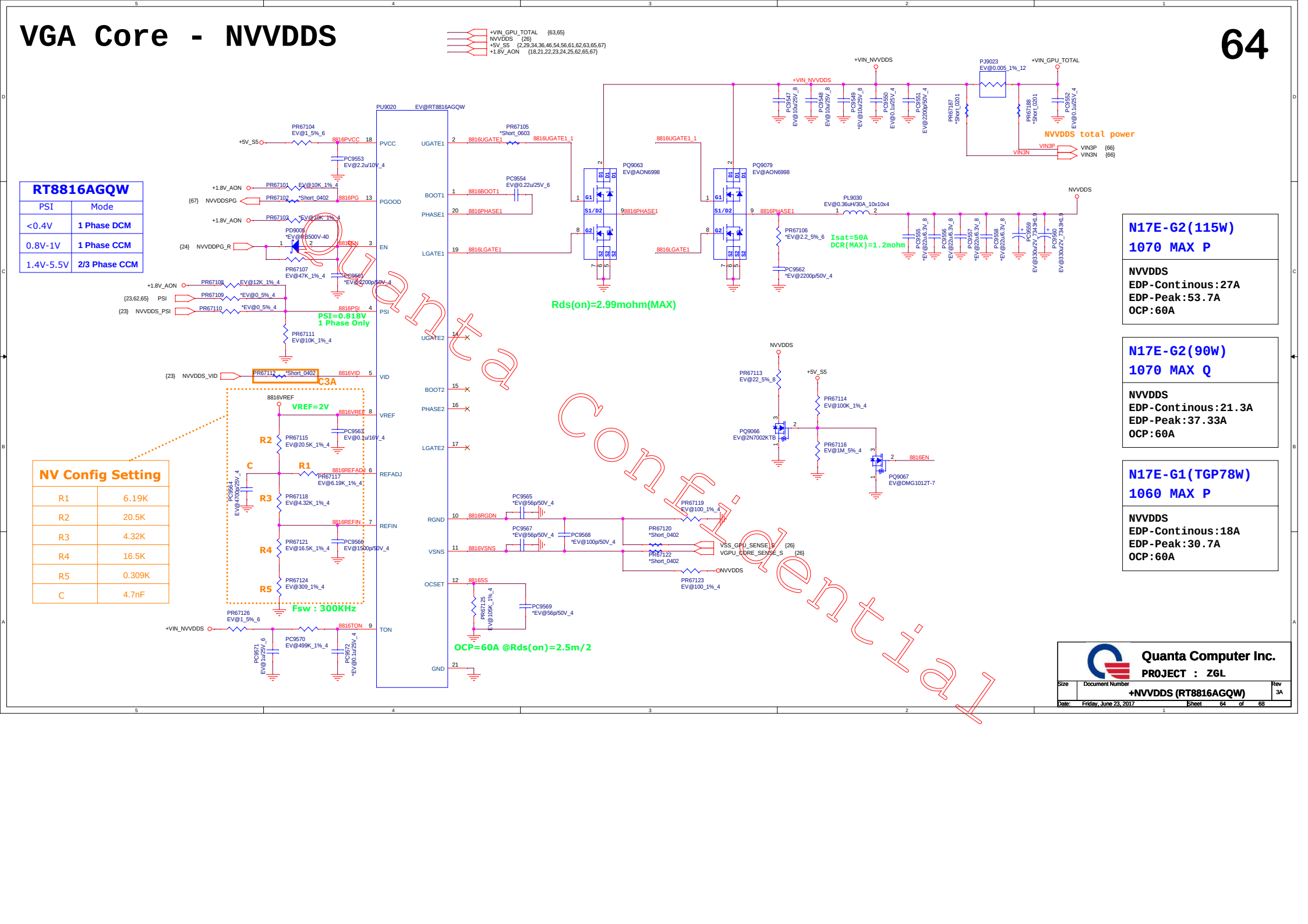
VGA Core - NVVDDS



RT8816AGQW	
PSI	Mode
<0.4V	1 Phase DCM
0.8V-1V	1 Phase CCM
1.4V-5.5V	2/3 Phase CCM

NV Config Setting	
R1	6.19K
R2	20.5K
R3	4.32K
R4	16.5K
R5	0.309K
C	4.7nF

N17E-G2(115W)
1070 MAX P

NVVDDS
EDP-Continous:27A
EDP-Peak:53.7A
OCP:60A

N17E-G2(90W)
1070 MAX Q

NVVDDS
EDP-Continous:21.3A
EDP-Peak:37.33A
OCP:60A

N17E-G1(TGP78W)
1060 MAX P

NVVDDS
EDP-Continous:18A
EDP-Peak:30.7A
OCP:60A

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Quanta Computer Inc.
PROJECT : ZGL
Size | Document Number: +NVVDDS (RT8816AGQW) | Rev: 3A
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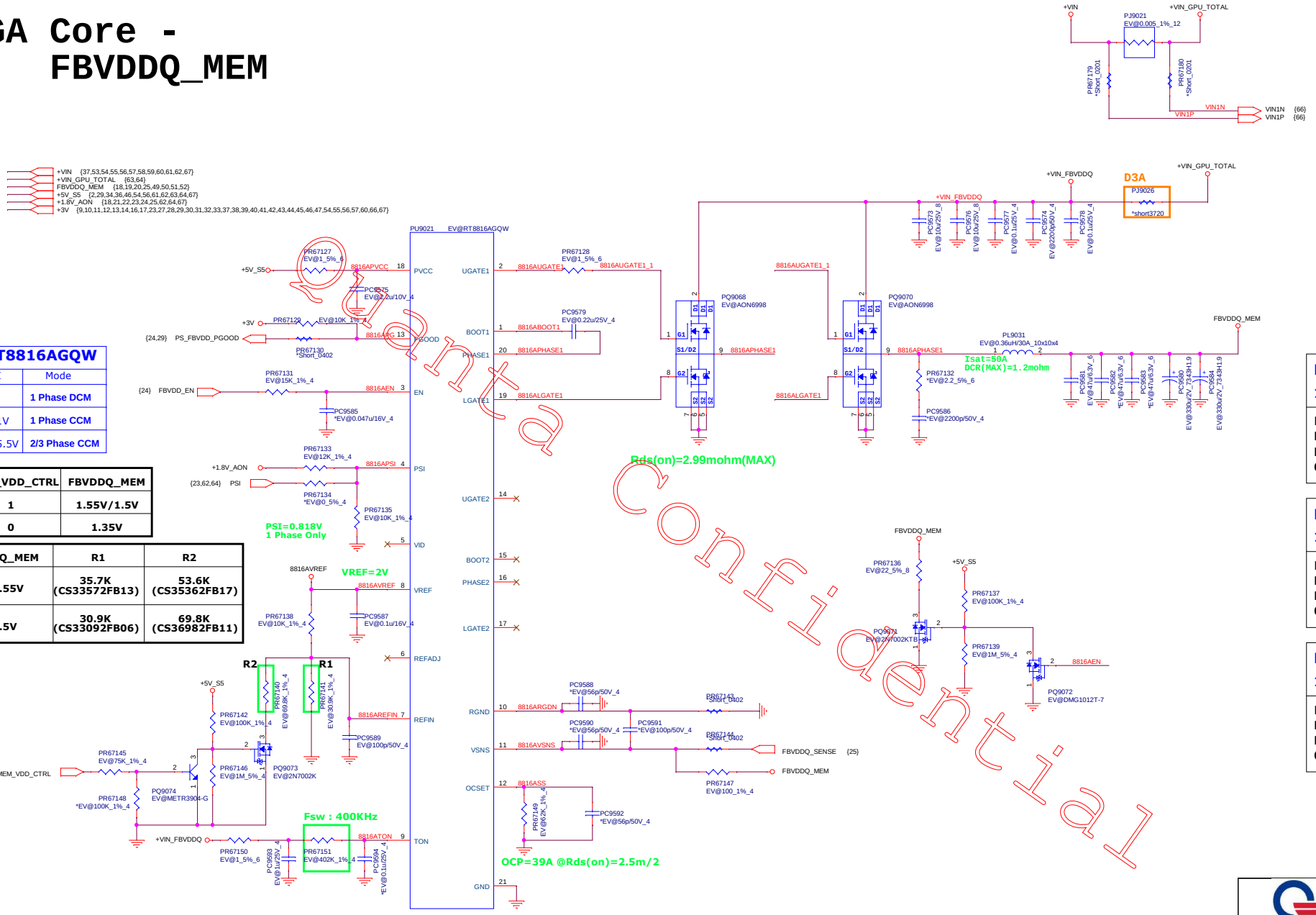
VGA Core - FBVDDQ_MEM



RT8816AGQW	
PSI	Mode
<0.4V	1 Phase DCM
0.8V-1V	1 Phase CCM
1.4V-5.5V	2/3 Phase CCM

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.55V/1.5V
0	1.35V

FBVDDQ_MEM	R1	R2
1.55V	35.7K (CS33572FB13)	53.6K (CS35362FB17)
1.5V	30.9K (CS33092FB06)	69.8K (CS36982FB11)

N17E-G2(115W)
1070 MAX P

FBVDDQ_MEM
EDP-Continous:25A
EDP-Peak:30.6A
OCP:39A

N17E-G2(90W)
1070 MAX Q

FBVDDQ_MEM
EDP-Continous:25A
EDP-Peak:30.6A
OCP:39A

N17E-G1(TGP78W)
1060 MAX P

FBVDDQ_MEM
EDP-Continous:19.8A
EDP-Peak:32.2A
OCP:39A

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	+FBVDDQ_MEM (RT8816AGQW)	3A

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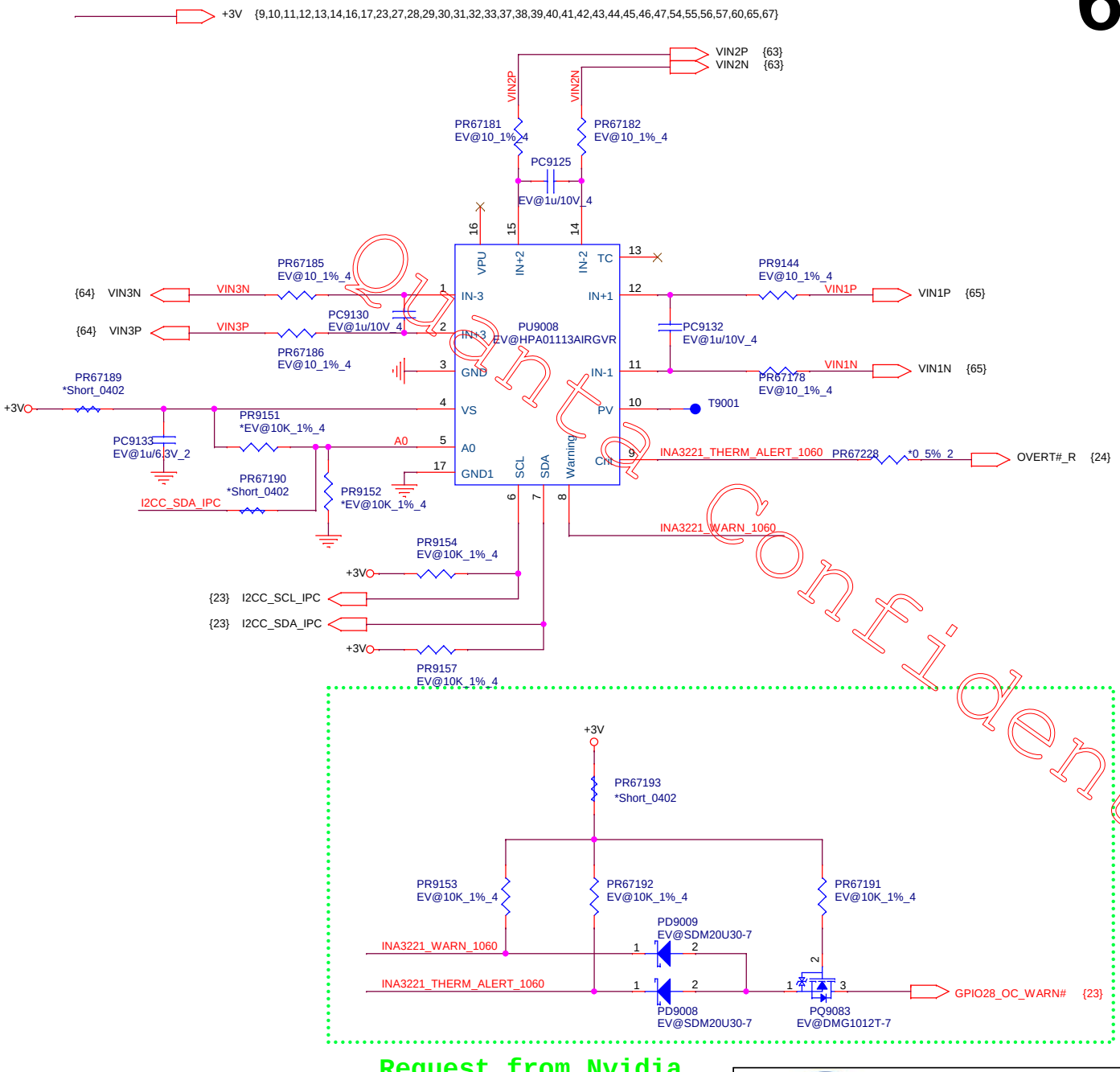

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Request from Nvidia

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+1.8V_S5 {60}
+1.8V_MAIN {18,24,25,30}
+1.8V_AON {18,21,22,23,24,25,62,64,65}
+5VPCU {10,34,36,37,45,46,54,55}

TDC : 0.08A
PEAK : 0.1A
Width : 20mil

TDC : 2.19A
PEAK : 2.92A
Width : 100mil

+1.8V_S5
PR67152 *Short_0805
PR67153 *Short_0805
D3A
PC9595 EV@1u/25V_4
PC9596 EV@1u/25V_4
+1.8V_MAIN
PR67154 *Short_0805
1V8_MAIN_S
PC9597 EV@10u/6.3V_6
PC9598 EV@0.1u/16V_4
PU9022 EV@AOZ1331DI
VIN1#1 VIN1#2 VIN2#1 VIN2#2
VOUT1#1 VOUT1#2
OUT2#1 OUT2#2
VBIAS
GND#1 GND#2
ON1 ON2 CT1 CT2
+5VPCU
PR67156 *Short_0402
PC9601 EV@0.1u/16V_4
PC9599 EV@0.1u/16V_4
PC9600 EV@10u/6.3V_6
1V8_AON_S
PR67155 *Short_0805
+1.8V_AON
PR67158 *Short_0402
PR67157 *Short_0402
{23,24,62} 1V8_MAIN_EN
1V8_AON_EN {24}
PC9602 *EV@820p/50V_4
PC9603 *EV@0.1u/16V_4
PC9604 *EV@1000p/50V_4
PC9605 *EV@1000p/50V_4

+VIN
PR67230 EV@1M_5%_6
PR67231 EV@22_5%_8
1V8_MAIN_EN
PQ9084 EV@LTC044EUBFS8TL
PR67232 EV@1M_5%_6
PQ9085 EV@2N7002KW
PR67233 *EV@100K_1%_6

+1.2VSUS {2,6,10,16,17,56}
+1V_GFX {18,21}
+5V_S5 {2,29,34,36,46,54,56,61,62,63,64,65}
+3V {9,10,11,12,13,14,16,17,23,27,28,29,30,31,32,33,37,38,39,40,41,42,43,44,45,46,47,54,55,56,57,60,65,66}

TDC : 1.52A
PEAK : 2.02A
Width : 80mil

+1.2VSUS
PJ9017 *Short_0603
PQ9075 EV@AON7408
PC9606 EV@0.1u/16V_4
PC9607 EV@10u/6.3V_6
9336DRV
+1V_GFX_S
PC9608 EV@10u/6.3V_6
PC9609 EV@10u/6.3V_6
PC9610 EV@0.1u/16V_4
+1V_GFX
PJ9018 *short3720
PC9611 *EV@220u/2V_7343H1.9
PR67159 EV@5.6_5%_8
+5V_S5
PR67160 EV@100K_1%_4
PQ9077 EV@DMG1012T-7
PR67163 EV@10K_5%_4
+3V
PR67161 EV@10K_1%_4
PQ9076 EV@2N7002K
PD9006 EV@1SS355
PQ9078 EV@2N7002K
+1.8V_AON
PR67162 EV@10K_1%_4
PU9023 EV@G9336ADJTP1U
PGD EN VCC GND DRV ADJ
{24} +1V_GFX_PG
PR67164 *Short_0402
PR67165 *Short_0402
{64} NVVDDSPG
PR67166 EV@47_1%_4
PC9612 EV@0.01u/50V_4
PR67167 EV@100_1%_4
9336ADJ
R1
R2
PR67169 EV@100_1%_4
+1V_GFX_S
Vout1=(1+R1/R2)*0.5
=1V
+5V_S5
PC9613 EV@0.1u/16V_4
1V8_AON_EN
PC9614 *EV@0.1u/16V_4
PR67168 *EV@0_5%_4

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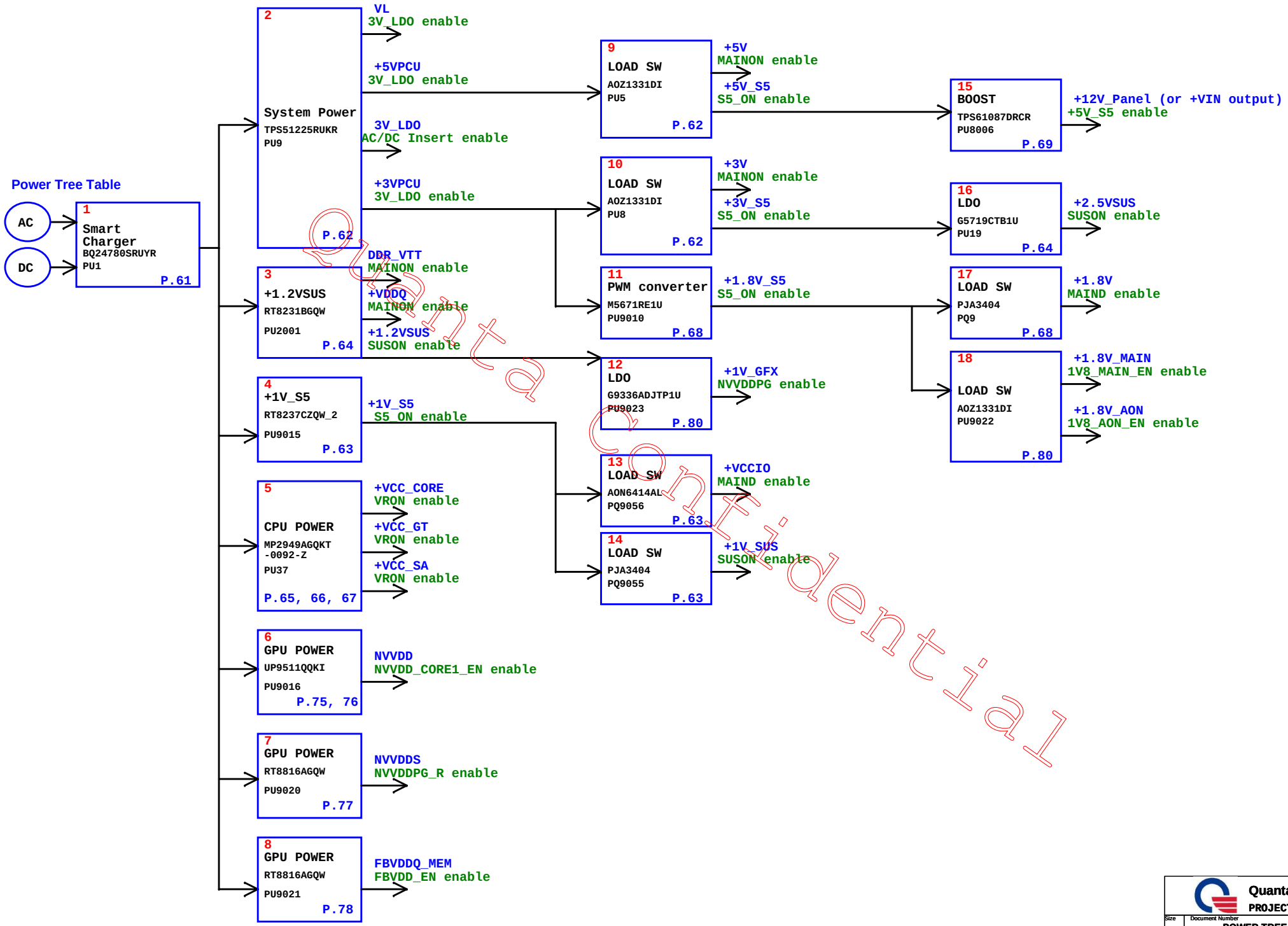

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